

Model Name: PANDA(MTQ45MK-LE)

| SHEET | TITLE                               |
|-------|-------------------------------------|
| 01    | COVER SHEET                         |
| 02    | BOM & PCB MODIFY HISTORY            |
| 03    | LGA775_A                            |
| 04    | LGA775_B                            |
| 05    | LGA775_C                            |
| 06    | LGA775_D                            |
| 07    | GMCH-HOST,PCIE,DMI                  |
| 08    | GMCH-DDRIII                         |
| 09    | GMCH-VGA,MISC                       |
| 10    | GMCH-GND                            |
| 11    | GMCH-POWER                          |
| 12    | DDRIII CHANNEL A                    |
| 13    | DDRIII CHANNEL B                    |
| 14    | DDRIII TERMINATION                  |
| 15    | SWITCH&DVI                          |
| 16    | PCIE SLOT X16,X1                    |
| 17    | ICH10-PCI,PCIE,USB,DMI              |
| 18    | ICH10-HOST,HDA,LAN,RTC,SPI,LPC,SATA |
| 19    | ICH10-POWER,GND                     |
| 20    | PCI SLOT                            |
| 21    | CKG IDT CV184                       |
| 22    | SIO SCH5617, TH, FDD                |
| 23    | COM, KB/MS, LPT                     |
| 24    | WPCT200AA, ST19WP18                 |
| 25    | FRONT PANEL,BUZZER                  |
| 26    | FRONT USB & REAL USB                |
| 27    | FAN CONTROL                         |

Revision 1.0

| SHEET | TITLE                       |
|-------|-----------------------------|
| 28    | DISCRETE POWER 1            |
| 29    | DISCRETE POWER 2            |
| 30    | VCORE PWM_NCP5392           |
| 31    | AUDIO CODEC                 |
| 32    | AUDIO JACK                  |
| 33    | ATX,SPI(BIOS),MECH HOLD     |
| 34    | INTEL 82567LM/LF            |
| 35    | NB&SB for GPIO LIST & STRAP |
| 36    | Other GPIO LIST & STRAP     |
| 37    | POWER DELIVERY              |
| 38    | POWER SEQUENCE              |
| 39    | BOM & PCB MODIFY HISTORY    |
| 40    |                             |
| 41    |                             |
| 42    |                             |

Example Fab Drawing Note

| Trace Width (mils) | Differential Spacing (mils) | Impedance            | Tolerance           |
|--------------------|-----------------------------|----------------------|---------------------|
| 4                  | NA                          | 50 ohm, single-ended | 15%                 |
| 6.5                | NA                          | 40 ohm, single-ended | 15%                 |
| 7.5                | NA                          | 37 ohm, single-ended | 15%                 |
| 9.5                | NA                          | 32 ohm, single-ended | 15%                 |
| 4                  | 8                           | 95 ohm, differential | 20%, reference only |
| 4.5                | 7.5                         | 90 ohm, differential | 20%, reference only |
| 5                  | 5                           | 85 ohm, differential |                     |

BEARLAKE Impedance Requirements by Interface

| Interface       | Impedance Required  |
|-----------------|---|
| FSB(ALL)        | 4x signals 42Ω others 50Ω, single-ended   |
| Controller Link | 50 ohm, single-ended  |
| PCI Express*2.0 | 85 ohm, single-ended  |
| DMI             | 95 ohm, differential  |
| VGA             | 37 ohm, single-ended at (G)MCH breakout, then 50 ohm single-ended to VGA connector. |

ICH10 Impedance Requirements by Interface

| Interface       | Impedance Required   |
|-----------------|----------------------|
| PCI             | 50 ohm, single-ended |
| Controller Link | 50 ohm, single-ended |
| Miscellaneous   | 50 ohm, single-ended |
| PCIE & DMI      | 95 ohm, differential |
| SATA            | 95 ohm, differential |
| USB             | 90 ohm, differential |

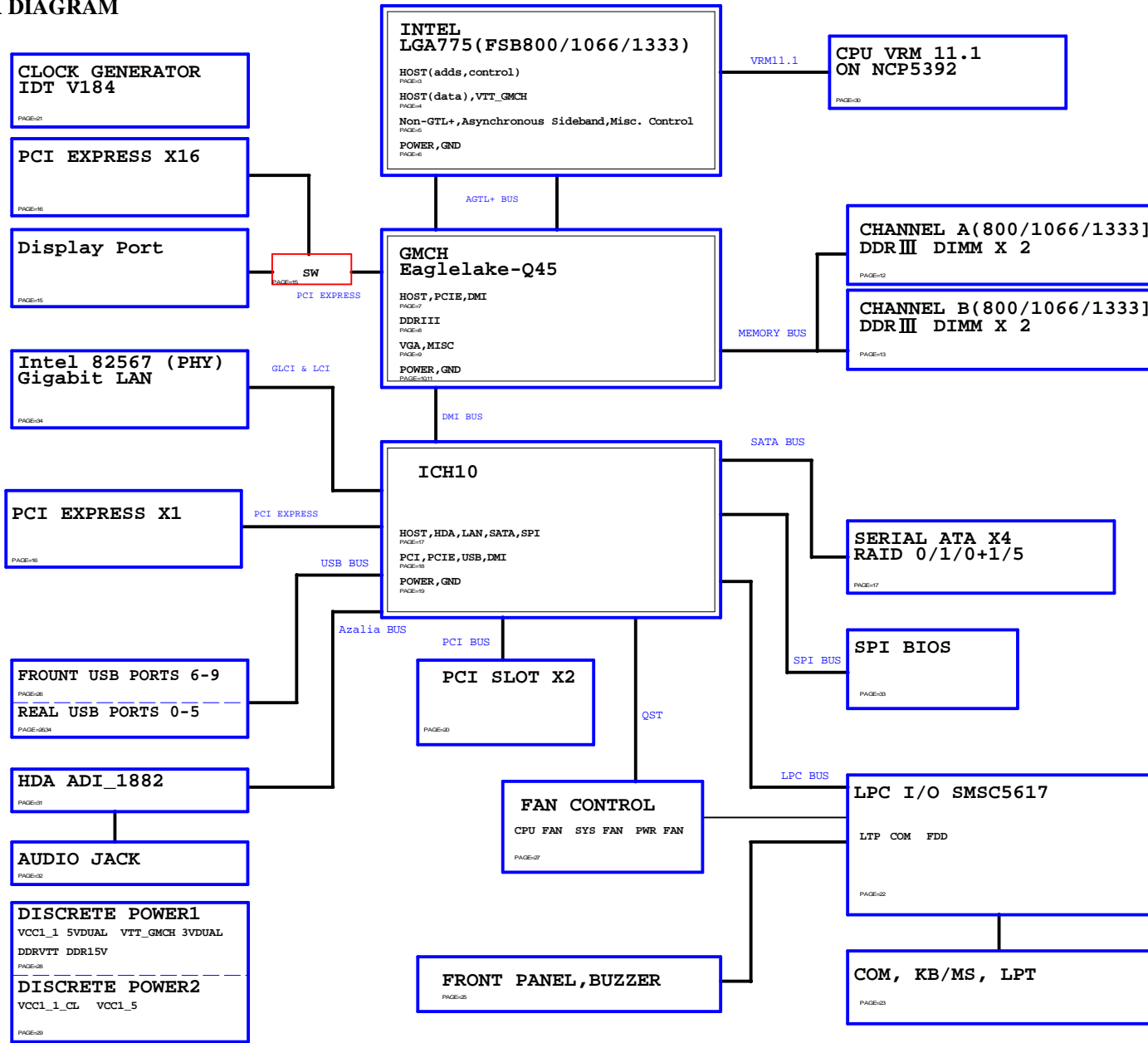
4-layer stack-up total thickness=59mils

|       |                |  |
|-------|----------------|--|
| ----- | SIGNAL LAYER   | 1.9 MILS (Final thickness after plating) |
| ----- | PREPREG 1080HR | 2.7 MILS                                 |
| ===== | VCC Layer      | 1.2 MILS (1 OZ COPPER)                   |
| ===== | CORE           | 47 MILS +/-5 mils                        |
| ===== | GND Layer      | 1.2 MILS (1 OZ COPPER)                   |
| ----- | PREPREG 1080HR | 2.7 MILS                                 |
| ----- | SIGNAL LAYER   | 1.9 MILS (Final thickness after plating) |

GIGABYTE TECHNOLOGIES, INC.

|                                 |                                |         |
|---------------------------------|--------------------------------|---------|
| Cover Sheet                     |                                |         |
| Size C                          | Document Number PANDA(MTQ45MK) | Rev 1.0 |
| Date: Thursday, August 21, 2008 | Sheet 1 of 39                  |         |

# BLOCK DIAGRAM



## LGA775A

LGA775  
(1/8)



CPU-SK/775/S/15



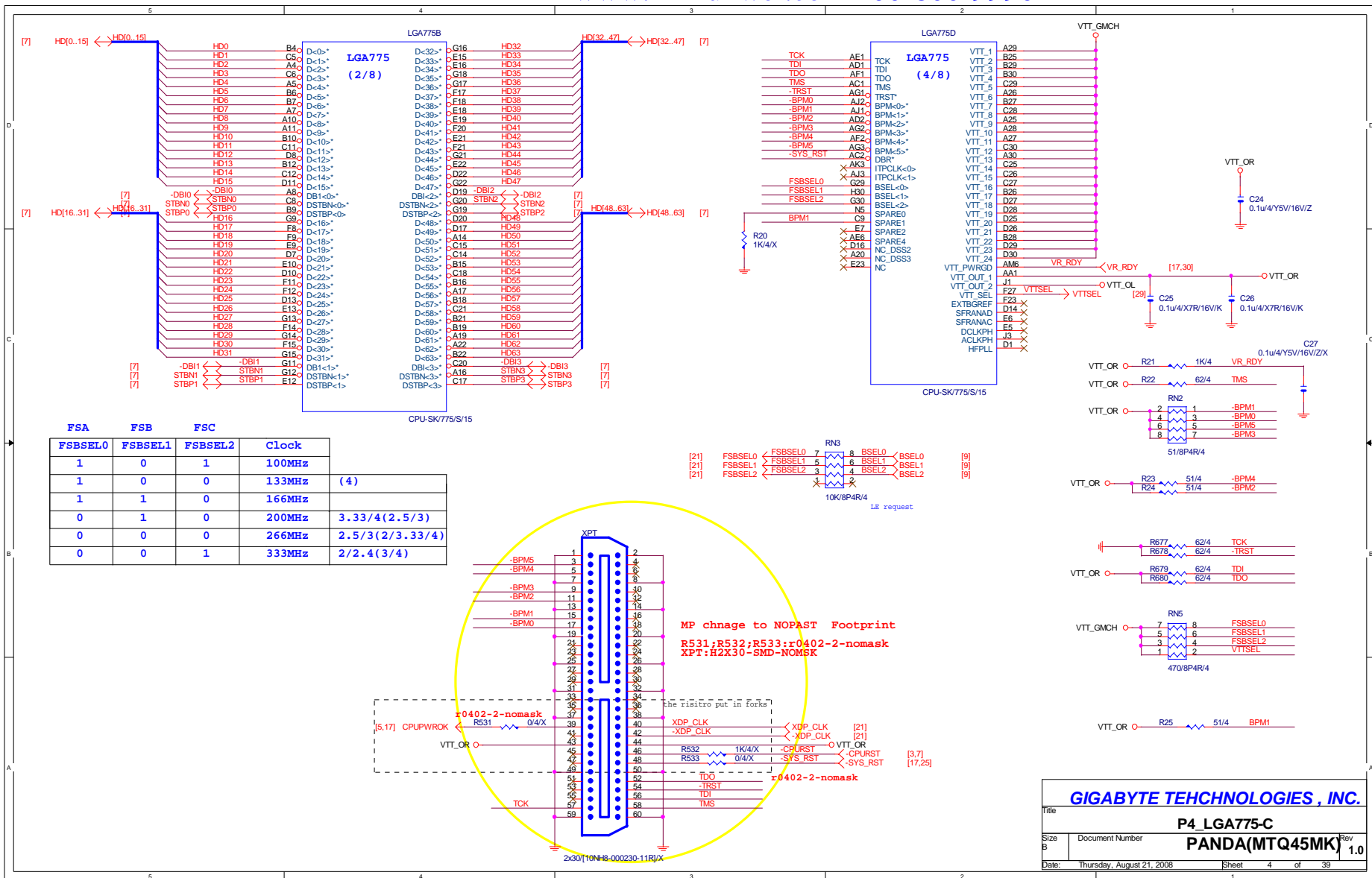
need remove GTLREF3&0 componet  
R10 change to 50/4/1

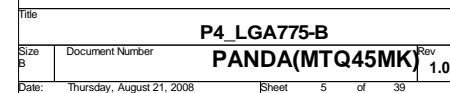
need remove GTLREF3&0 componet  
R10 change to 50/4/1

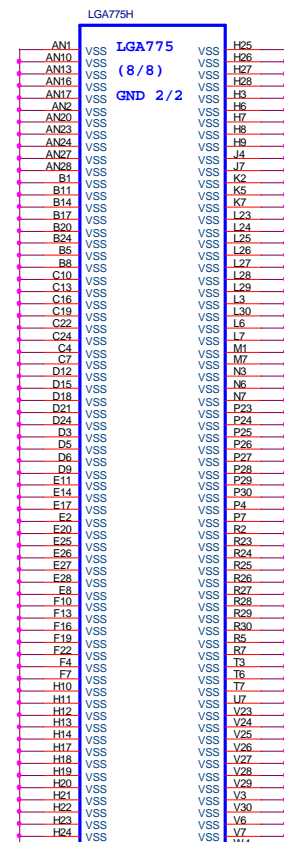


Figure 10 illustrates the test point connections for the CPURST, IERR, and BR0 signals. The diagram shows three input signals (VTT\_GMCH, VTT\_OR, VTT\_OL) connected to resistors R17, R18, and R19 (all 62/4) which then connect to the CPURST, IERR, and BR0 pins of the RN1 51/8P4R/4 component. The component also has test points 1, 2, 3, 4, 5, 6, 7, and 8 connected to TESTH8, TESTH9, and TESTH10 signals.

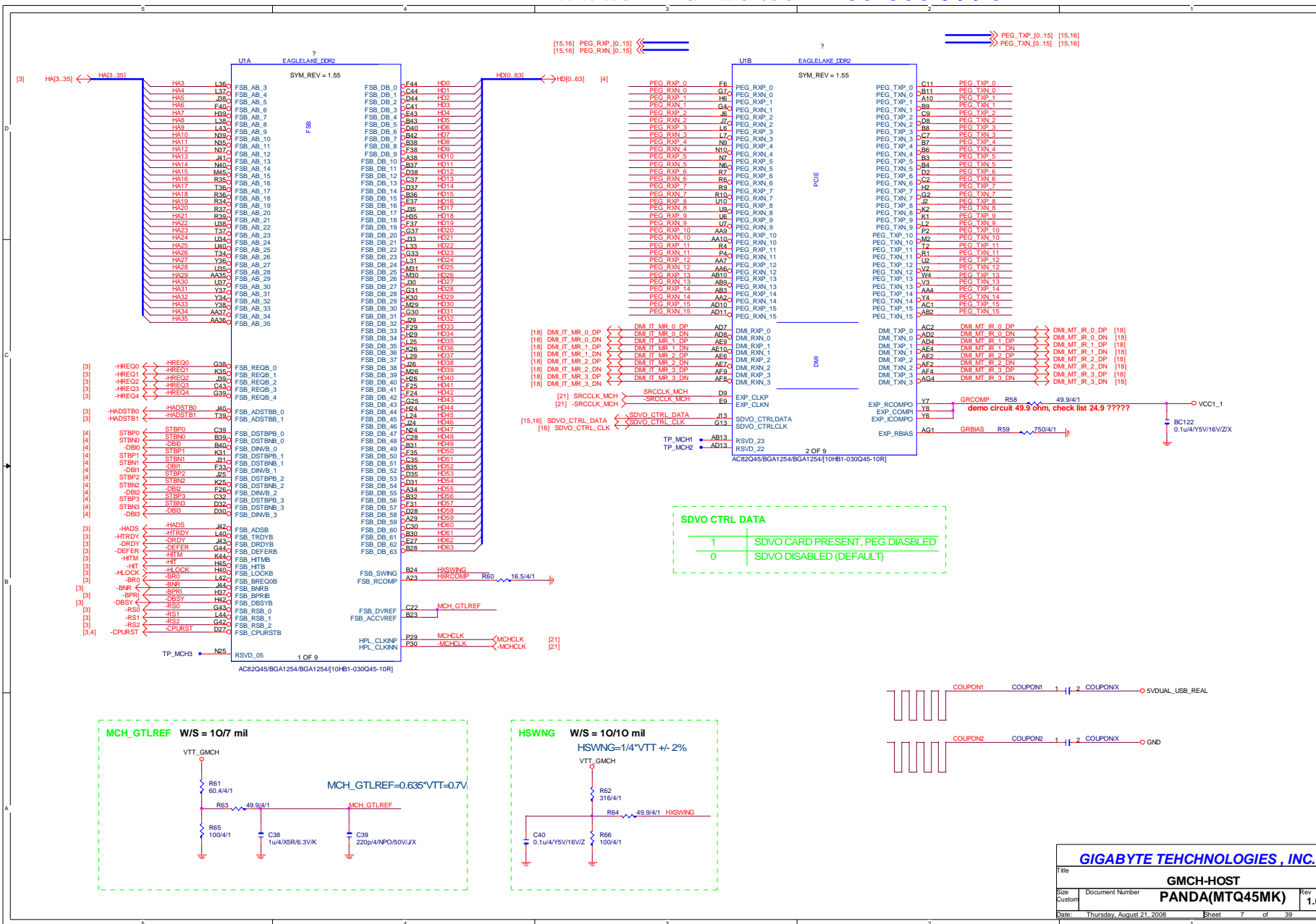
|                                 |                 |                |         |
|---------------------------------|-----------------|----------------|---------|
| Title                           |                 | P4_LGA775-A    |         |
| Size B                          | Document Number | PANDA(MTQ45MK) | Rev 1.0 |
| Date: Thursday, August 21, 2008 |                 | Sheet 3 of 39  |         |





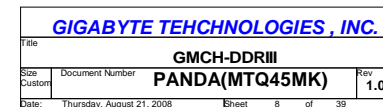


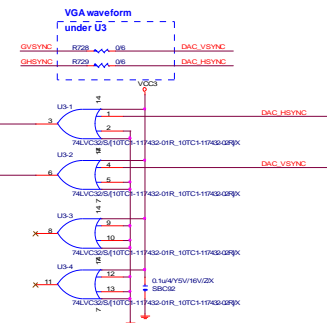
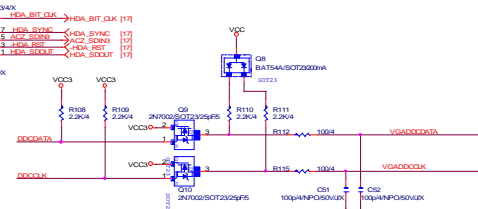
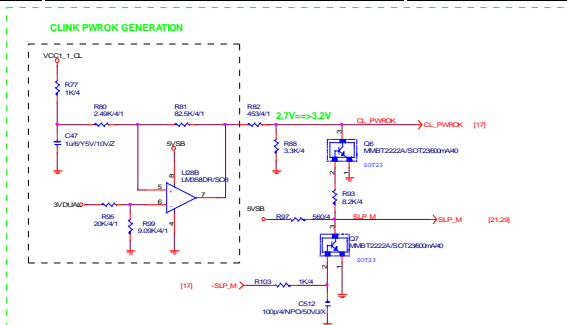
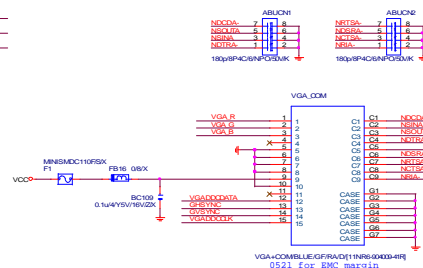
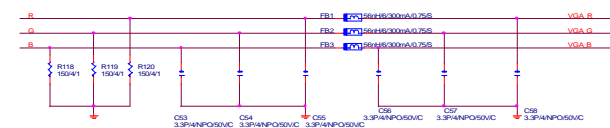
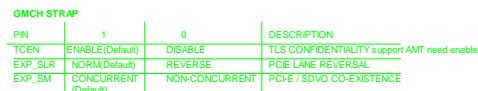
|        |                           |                |   |     |     |
|--------|---------------------------|----------------|---|-----|-----|
| Title  |                           | P4_LGA775-D    |   | Rev | 1.0 |
| Size B | Document Number           | PANDA(MTQ45MK) |   |     |     |
| Date:  | Thursday, August 21, 2008 | Sheet          | 6 | of  | 39  |

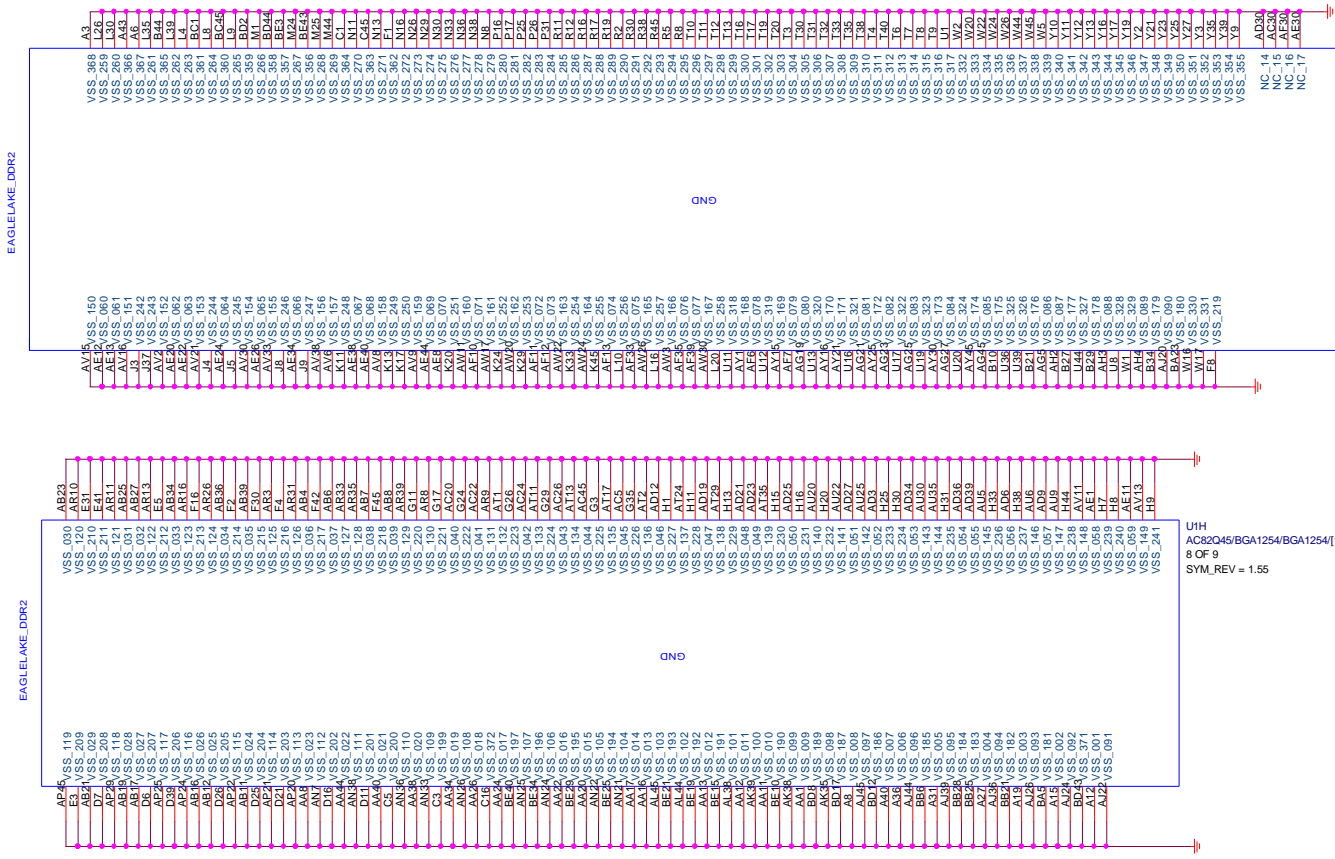


GIGABYTE TECHNOLOGIES, INC.

|        |                           |                |         |
|--------|---------------------------|----------------|---------|
| File   | GMCH-HOST                 | Rev            | 1.0     |
| Size   | Document Number           | PANDA(MTQ45MK) |         |
| Custom |                           |                |         |
| Date:  | Thursday, August 21, 2008 | Sheet          | 7 of 39 |

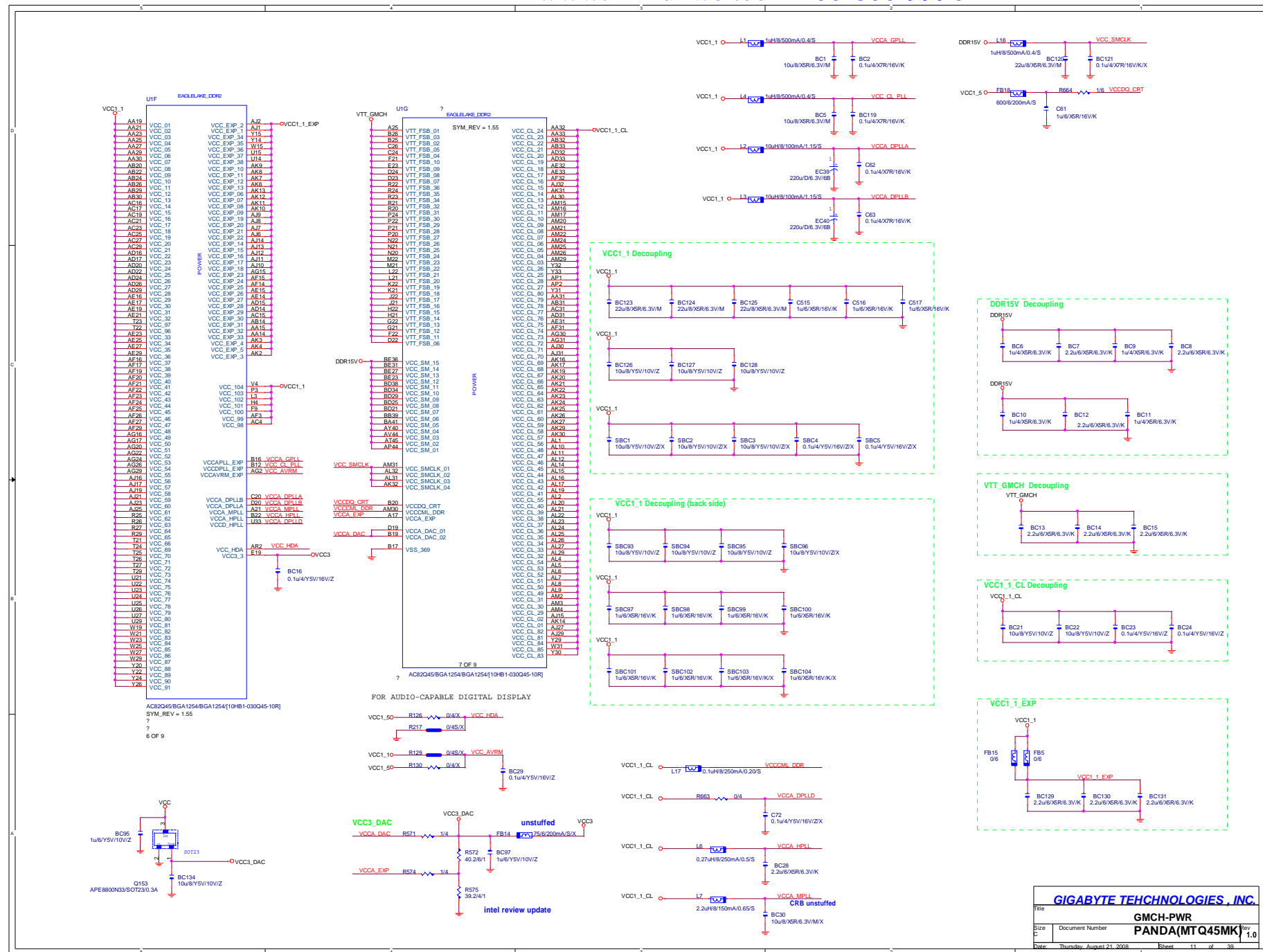


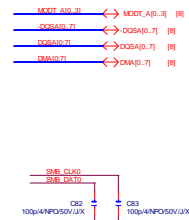
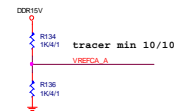
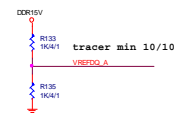
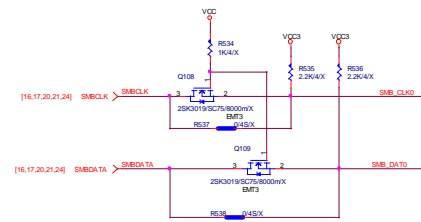
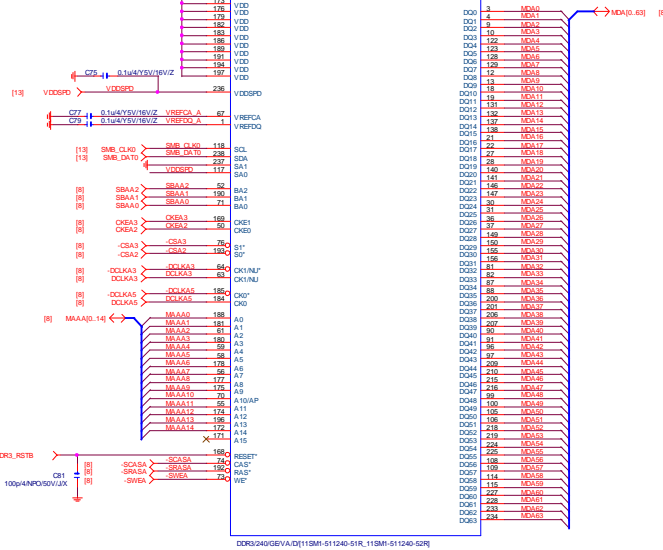


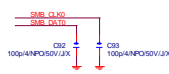
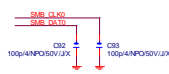


U11  
AC82045/BGA1254/BGA1254/[10H]B1-030Q45-10R  
9 OF 9  
SYM\_REV = 1.55

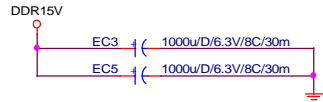
U11  
AC82045/BGA1254/BGA1254/[10H]B1-030Q45-10R  
8 OF 9  
SYM\_REV = 1.55



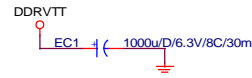
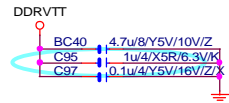




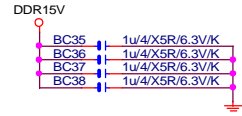
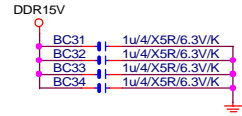
## CHANNEL A



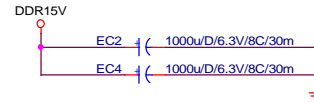
### DDRVTT Decouple



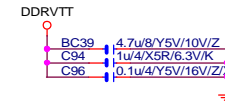
### DDR15V Decoupling



## CHANNEL B



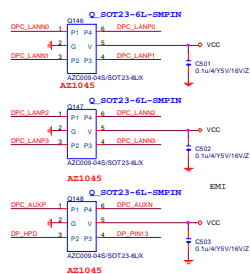
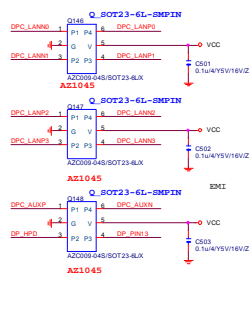
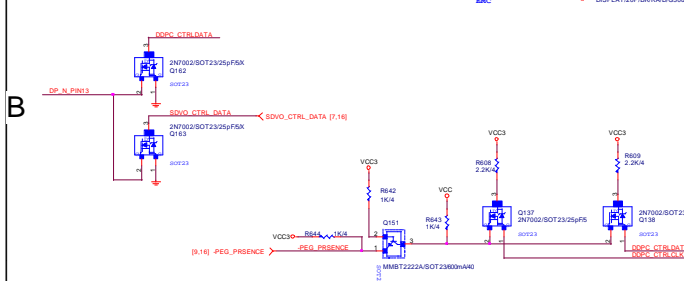
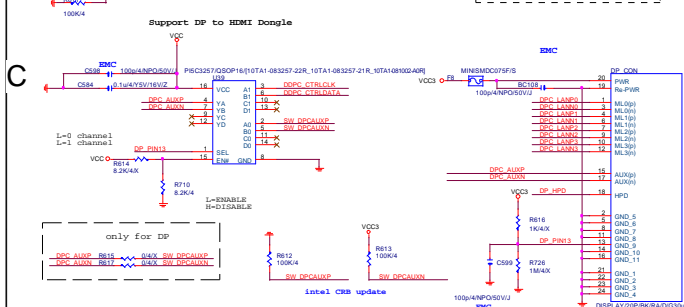
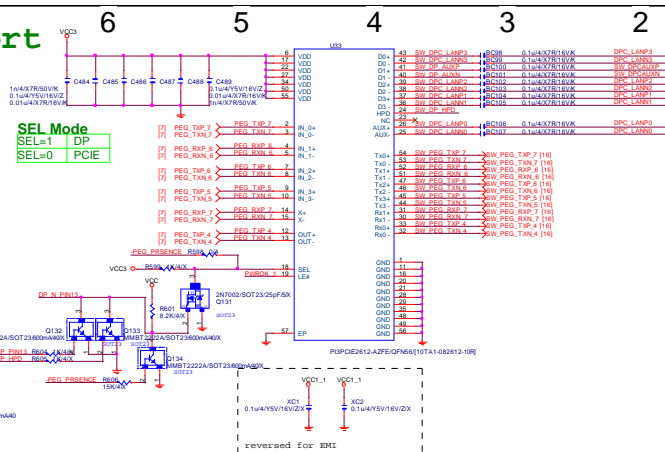
### DDRVTT Decouple

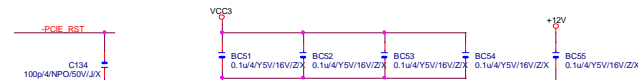
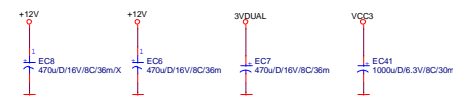
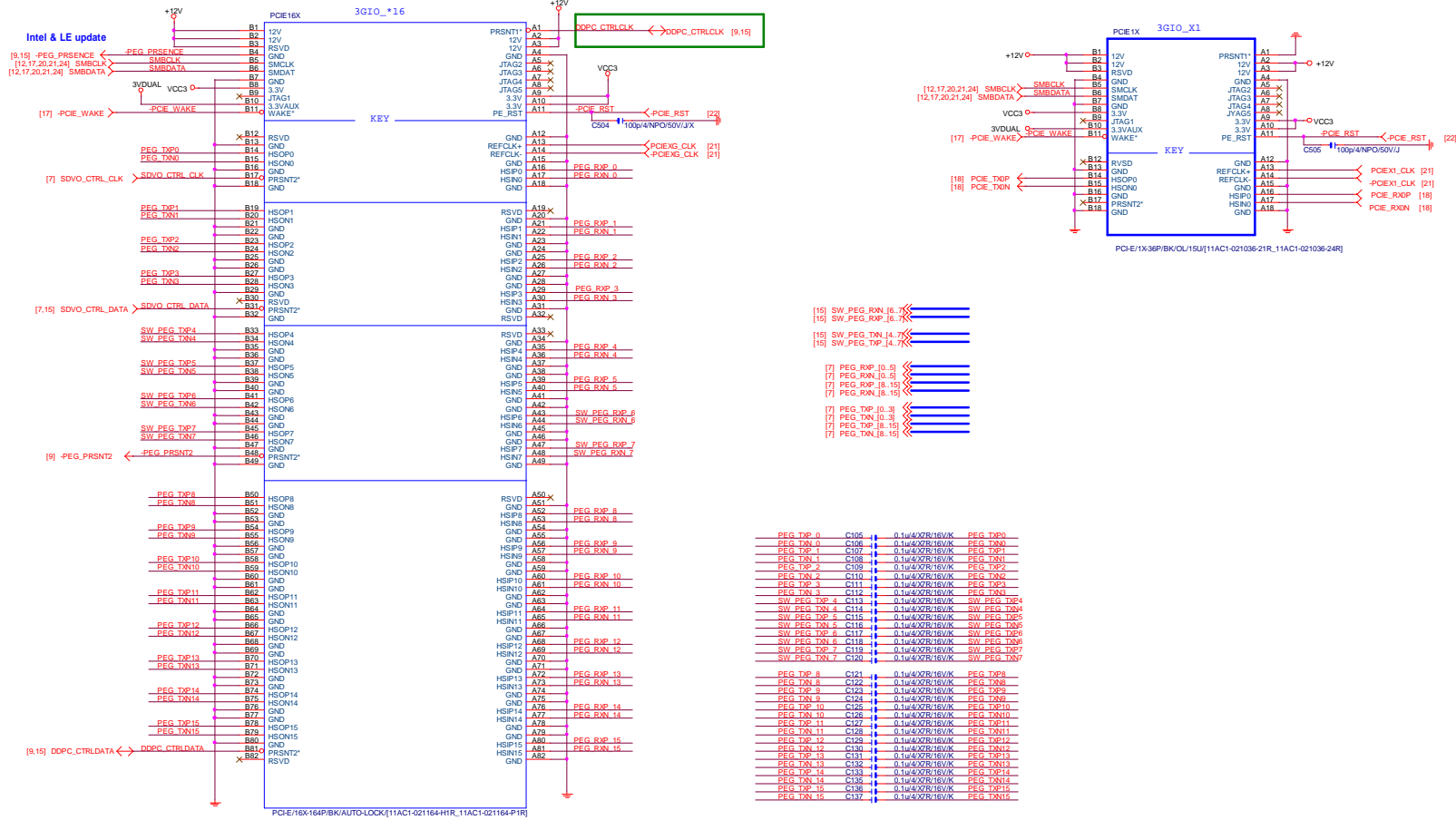


**GIGABYTE TECHNOLOGIES, INC.**

|                 |                           |                |
|-----------------|---------------------------|----------------|
| Title           |                           |                |
| DDR3 TERMINATOR |                           |                |
| Size            | Document Number           | Rev            |
| Custom          | PANDA(MTQ45MK)            | 1.0            |
| Date:           | Thursday, August 21, 2008 | Sheet 14 of 39 |

| Port C      |                |              |  |
|-------------|----------------|--------------|--|
| Strap       | D0PC_CTLRLDATA |              |  |
| PCI Express | DisplayPort    | HDMI/DP      |  |
| PEG_TXP_7   | DPC_LANE3      | TMDSC_CLK    |  |
| PEG_TXN_7   | DPC_LANE3#     | TMDSC_CLK#   |  |
| PEG_TXP_6   | DPC_LANE2      | TMDSC_DATA0  |  |
| PEG_TXN_6   | DPC_LANE2#     | TMDSC_DATA0# |  |
| PEG_TXP_5   | DPC_LANE1      | TMDSC_DATA1  |  |
| PEG_TXN_5   | DPC_LANE1#     | TMDSC_DATA1# |  |
| PEG_TXP_4   | DPC_LANE0      | TMDSC_DATA2  |  |
| PEG_TXN_4   | DPC_LANE0#     | TMDSC_DATA2# |  |
| PEG_RXP_7   | DPC_HPD        | TMDSC_HPD    |  |
| PEG_RXN_7   |                |              |  |
| PEG_RXP_6   | DPC_ALK        |              |  |
| PEG_RXN_6   | DPC_ALK#       |              |  |

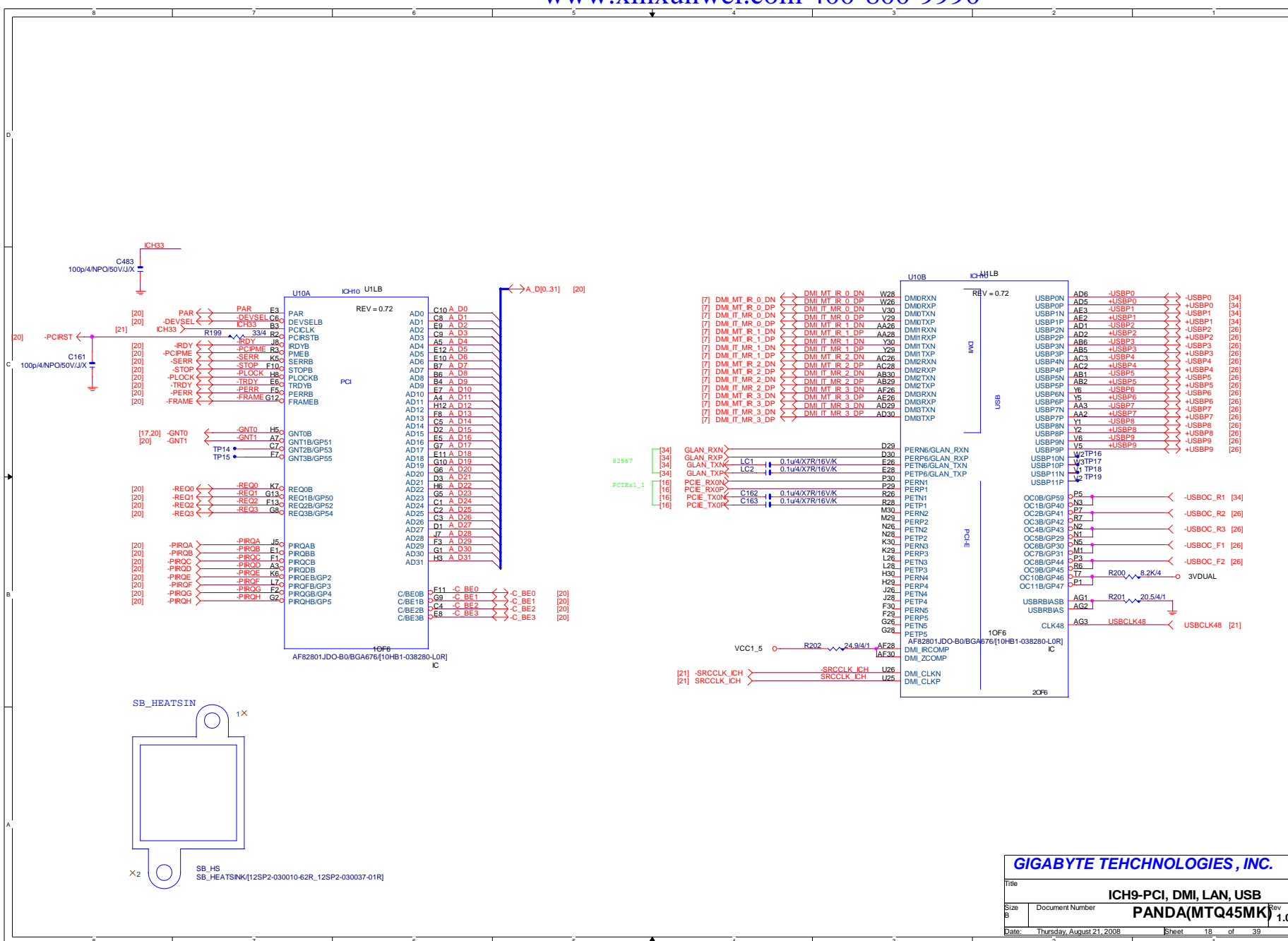


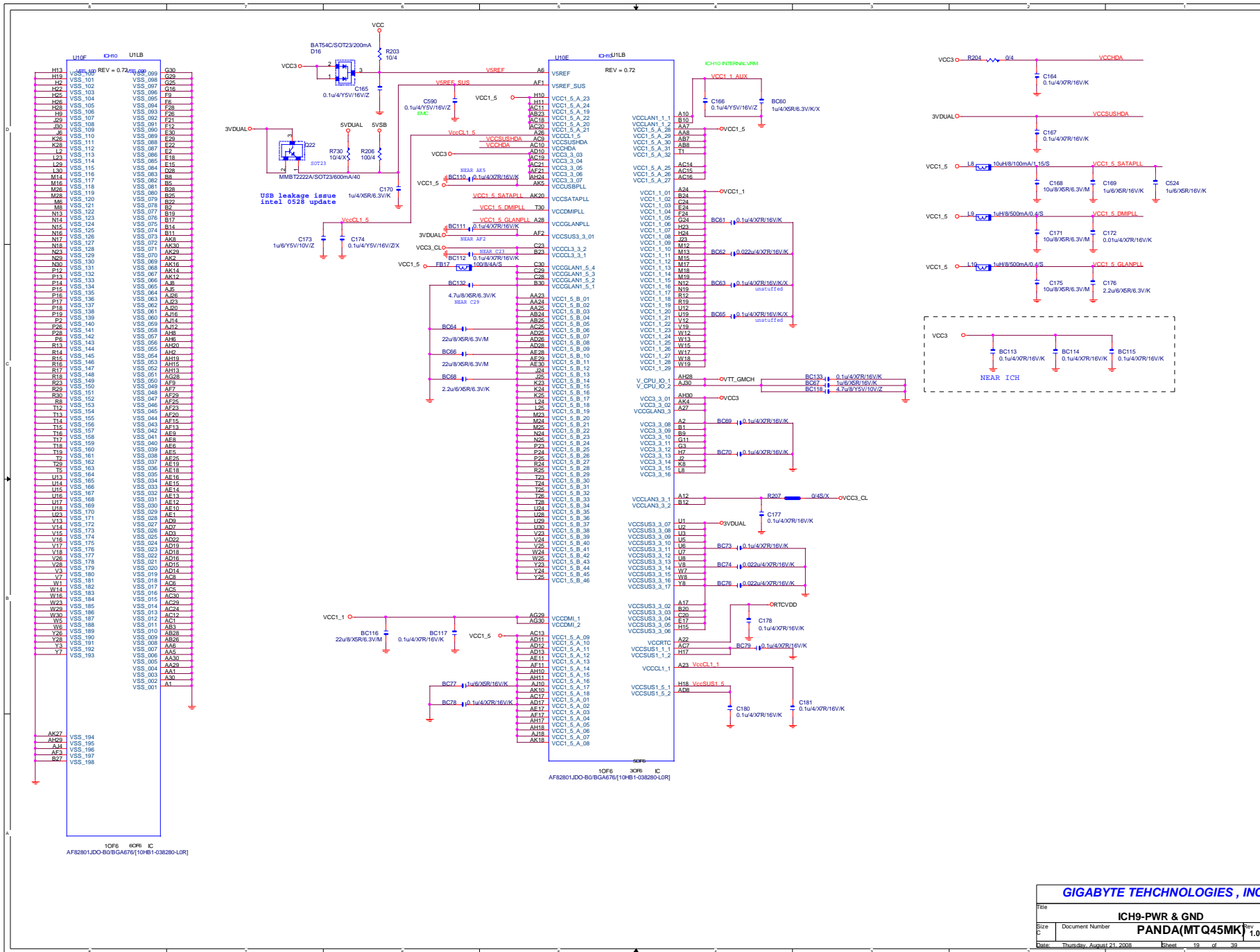


GIGABYTE TECHNOLOGIES, INC.

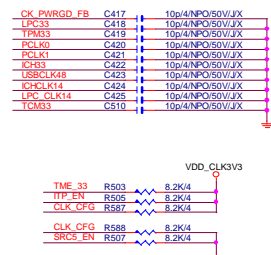
|      |                           |                |          |
|------|---------------------------|----------------|----------|
| File | PCI EXPRESS * 16_A        |                |          |
| Size | Document Number           | PANDA(MTQ45MK) |          |
| C    |                           | Rev 1.0        |          |
| Date | Thursday, August 21, 2008 | Sheet          | 16 of 38 |



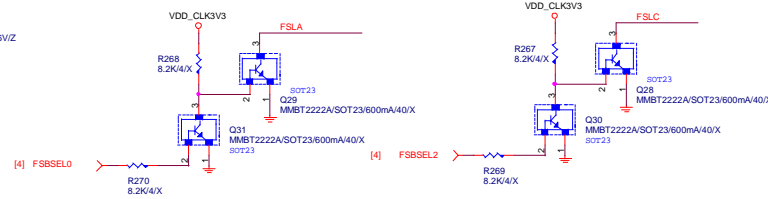
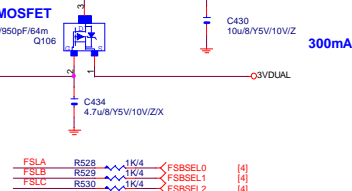
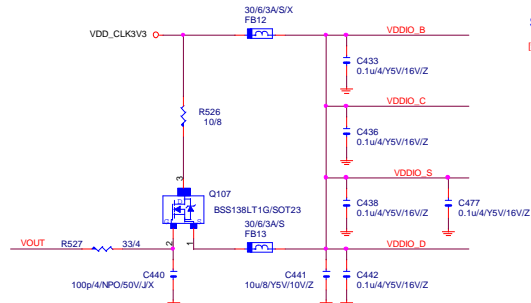


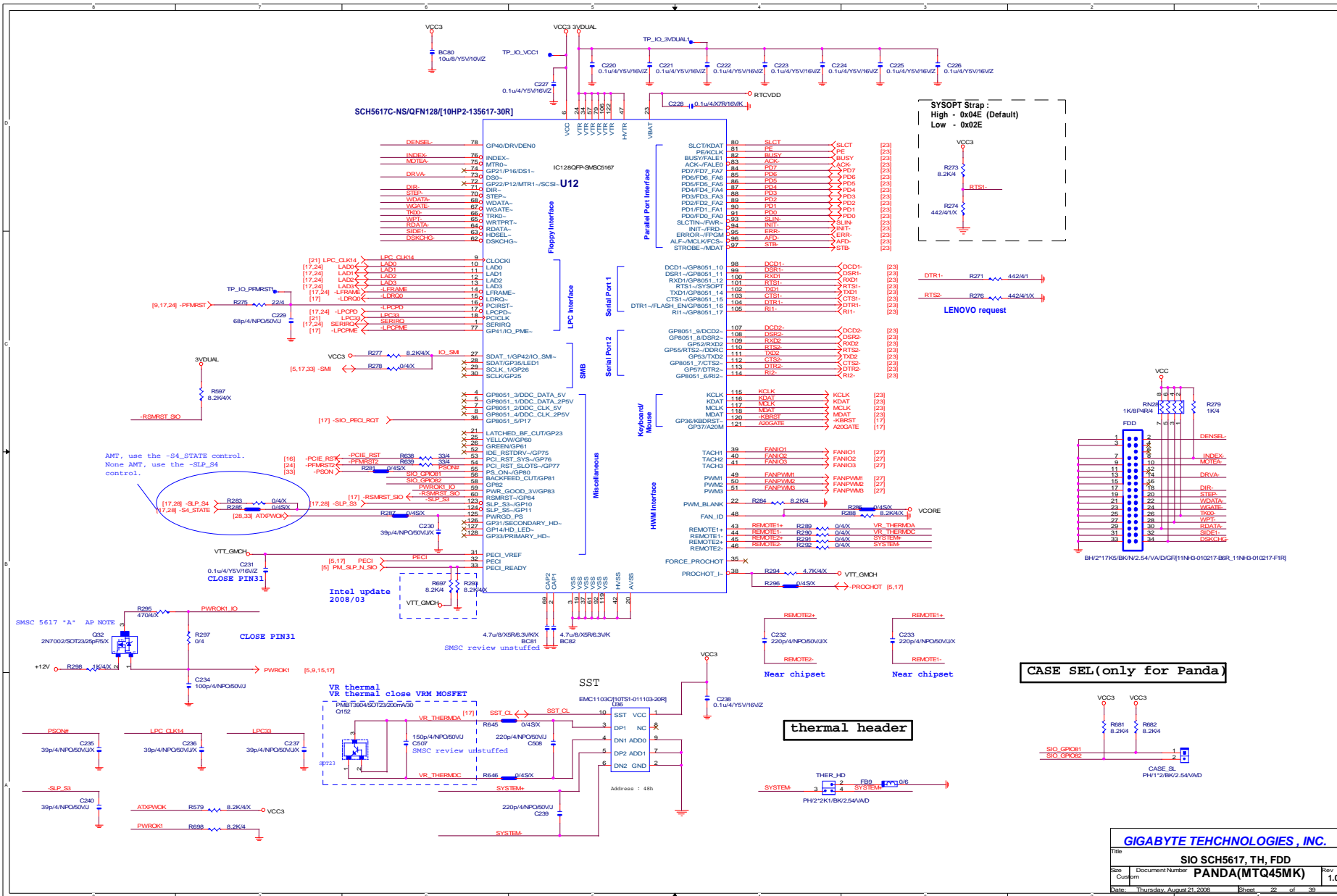




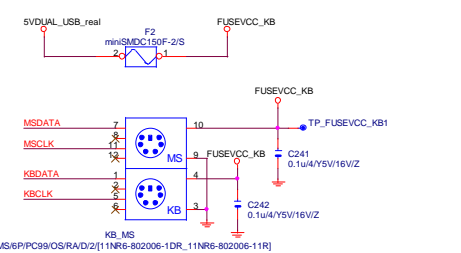
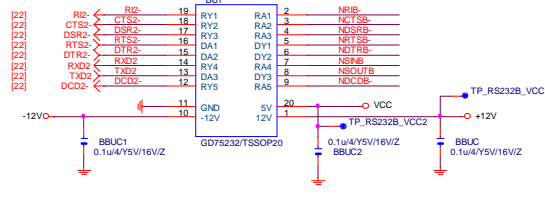
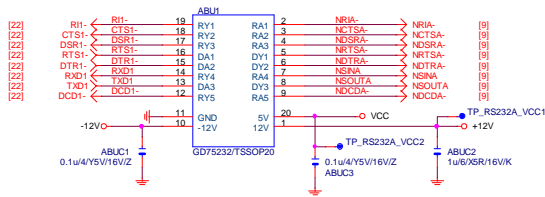


| FSC | FSB | FSA |    |
|-----|-----|-----|----|
| 0   | 0   | 0   | 26 |
| 0   | 0   | 1   | 13 |
| 0   | 1   | 0   | 20 |
| 0   | 1   | 1   | 16 |
| 1   | 0   | 0   | 33 |
| 1   | 0   | 1   | 10 |
| 1   | 1   | 0   | 40 |
| 1   | 1   | 1   | 20 |

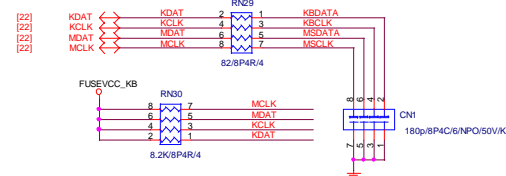
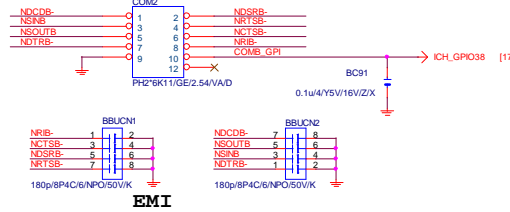
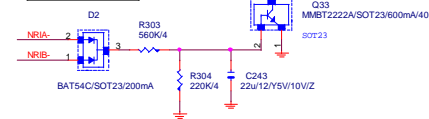




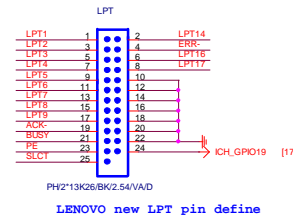
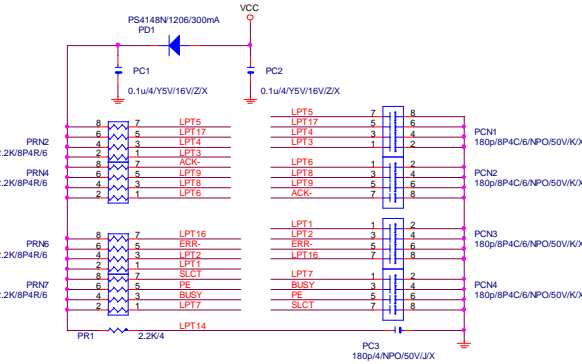
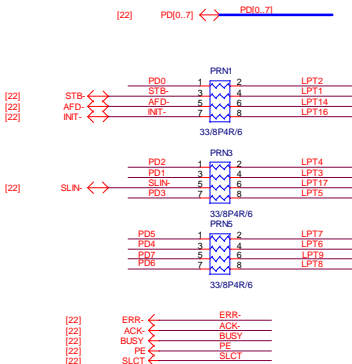
# COM



# RING IN



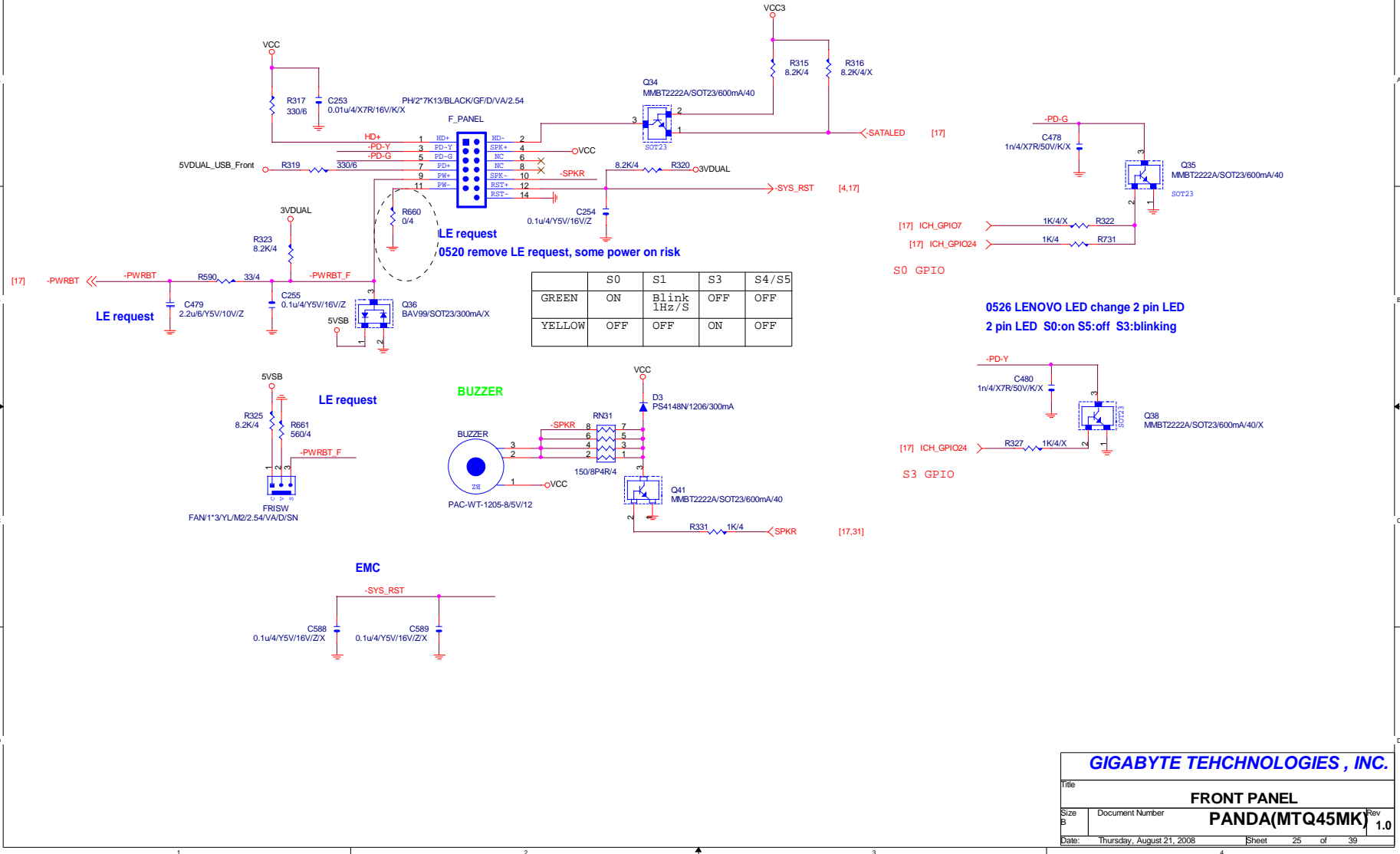
# LPT

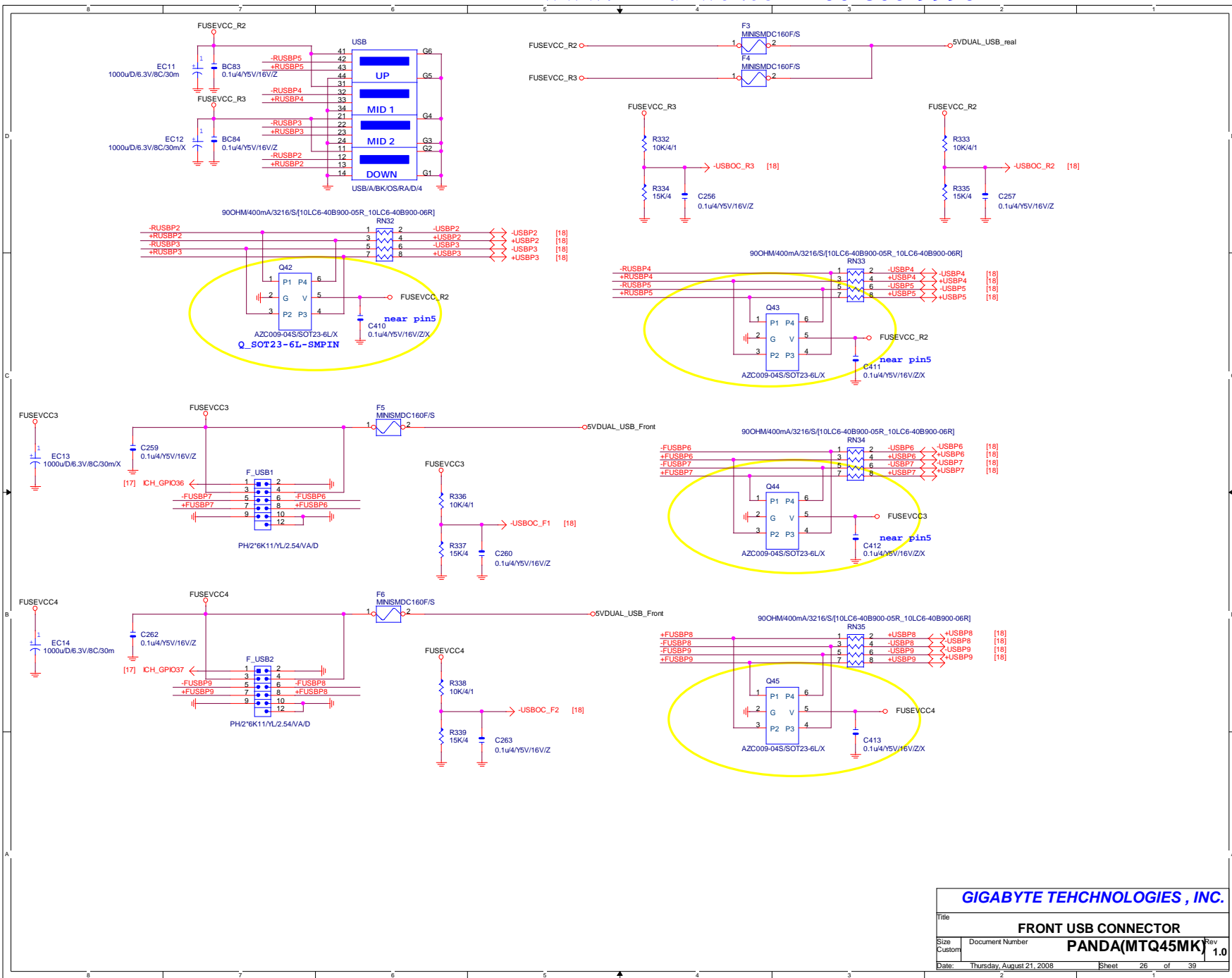


| GIGABYTE TECHNOLOGIES, INC. |                           |                |
|-----------------------------|---------------------------|----------------|
| COM, KB/MS, LPT             |                           |                |
| File                        | Document Number           | Rev            |
|                             | PANDA(MTQ45MK)            | 1.0            |
| Date:                       | Thursday, August 21, 2008 | Sheet 23 of 39 |



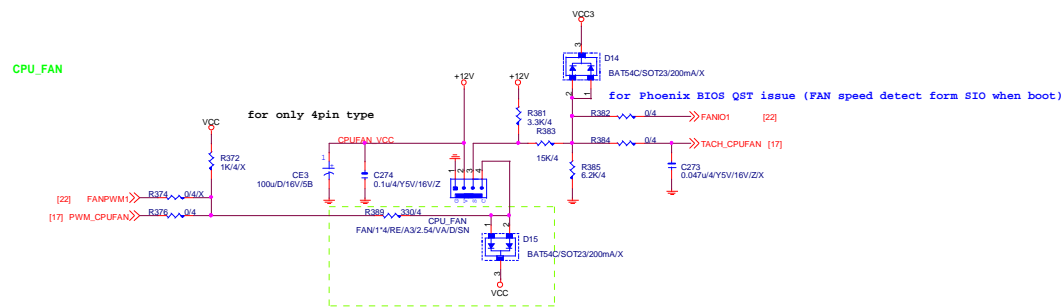
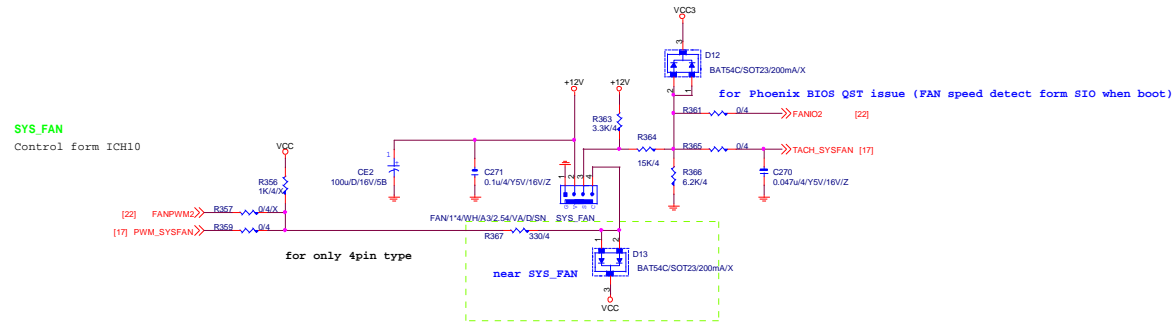
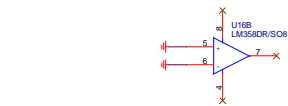
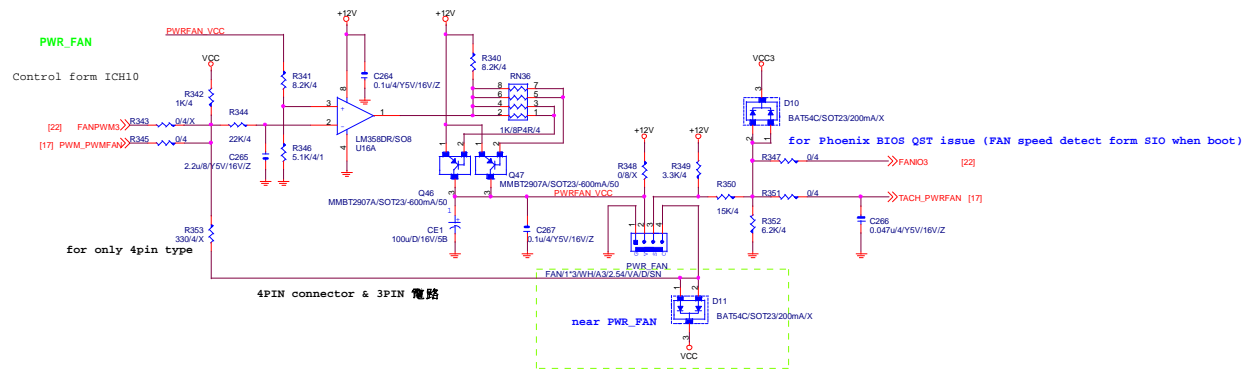
# INTEL FRONT PANEL





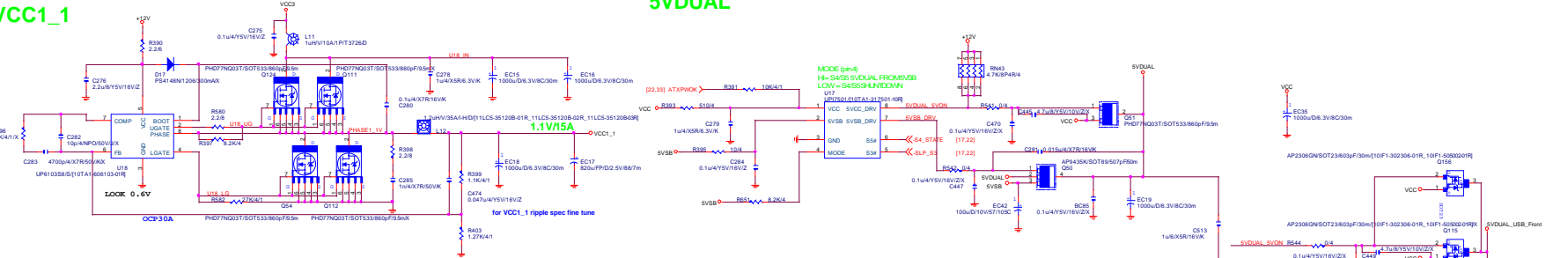
GIGABYTE TECHNOLOGIES, INC.

|        |                           |                        |          |
|--------|---------------------------|------------------------|----------|
| Title  |                           | FRONT USB CONNECTOR    |          |
| Size   | Document Number           | PANDA(MTQ45MK) Rev 1.0 |          |
| Custom |                           |                        |          |
| Date:  | Thursday, August 21, 2008 | Sheet                  | 26 of 39 |

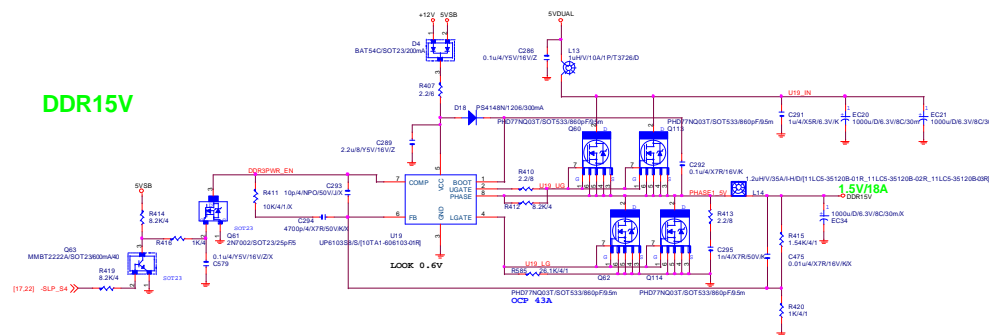


## VCC1\_1

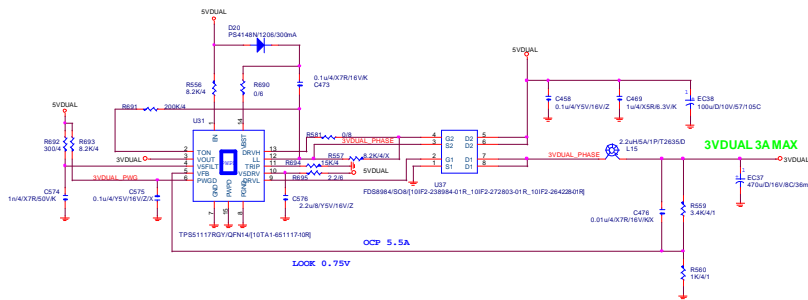
## 5VDUAL



## DDR15V

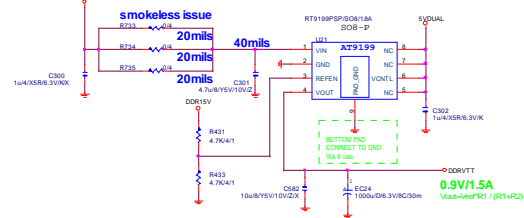


## 3VDUAL

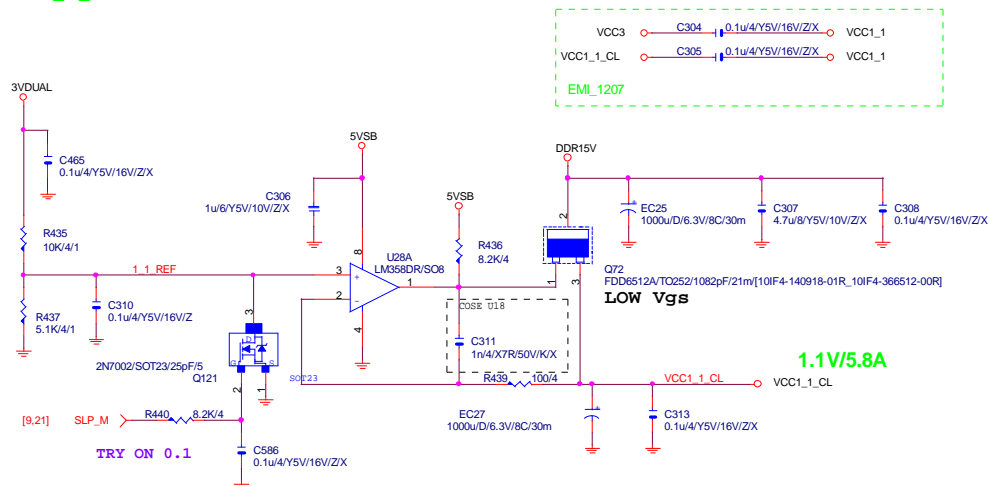


## DDRVT

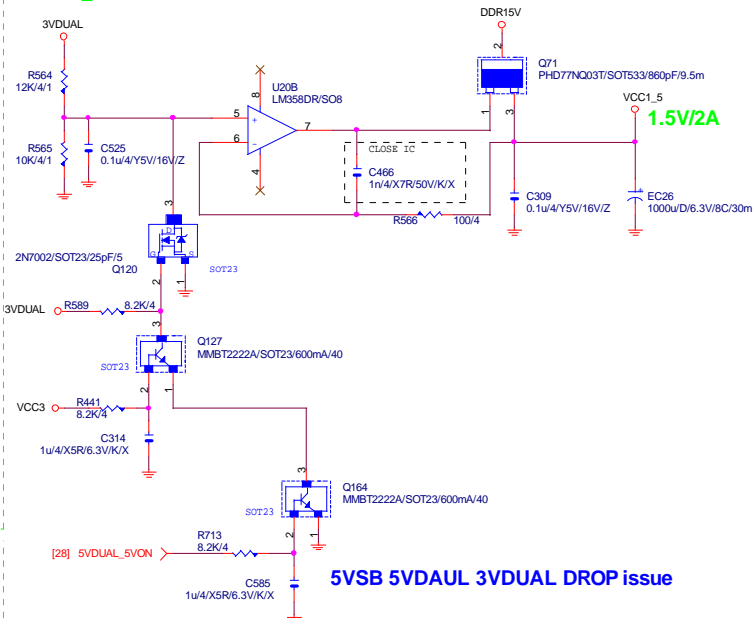
DDR3 0.75V/0.83A



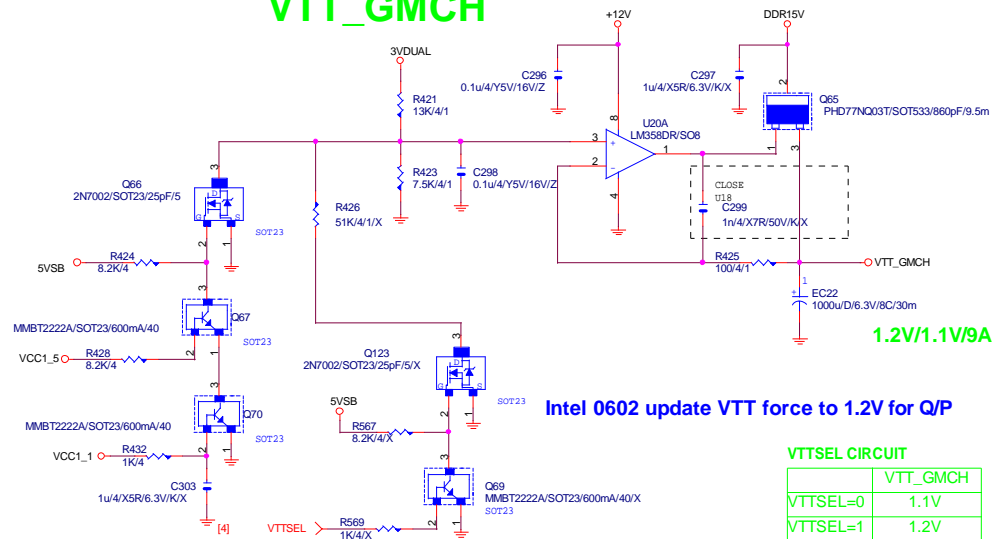
## VCC1\_1\_CL



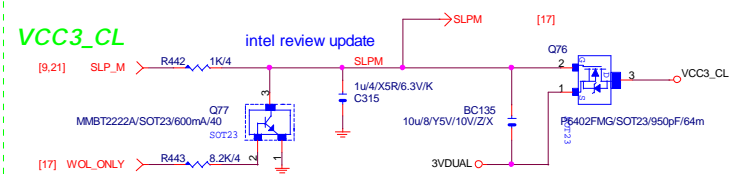
## VCC1\_5



## VTT\_GMCH

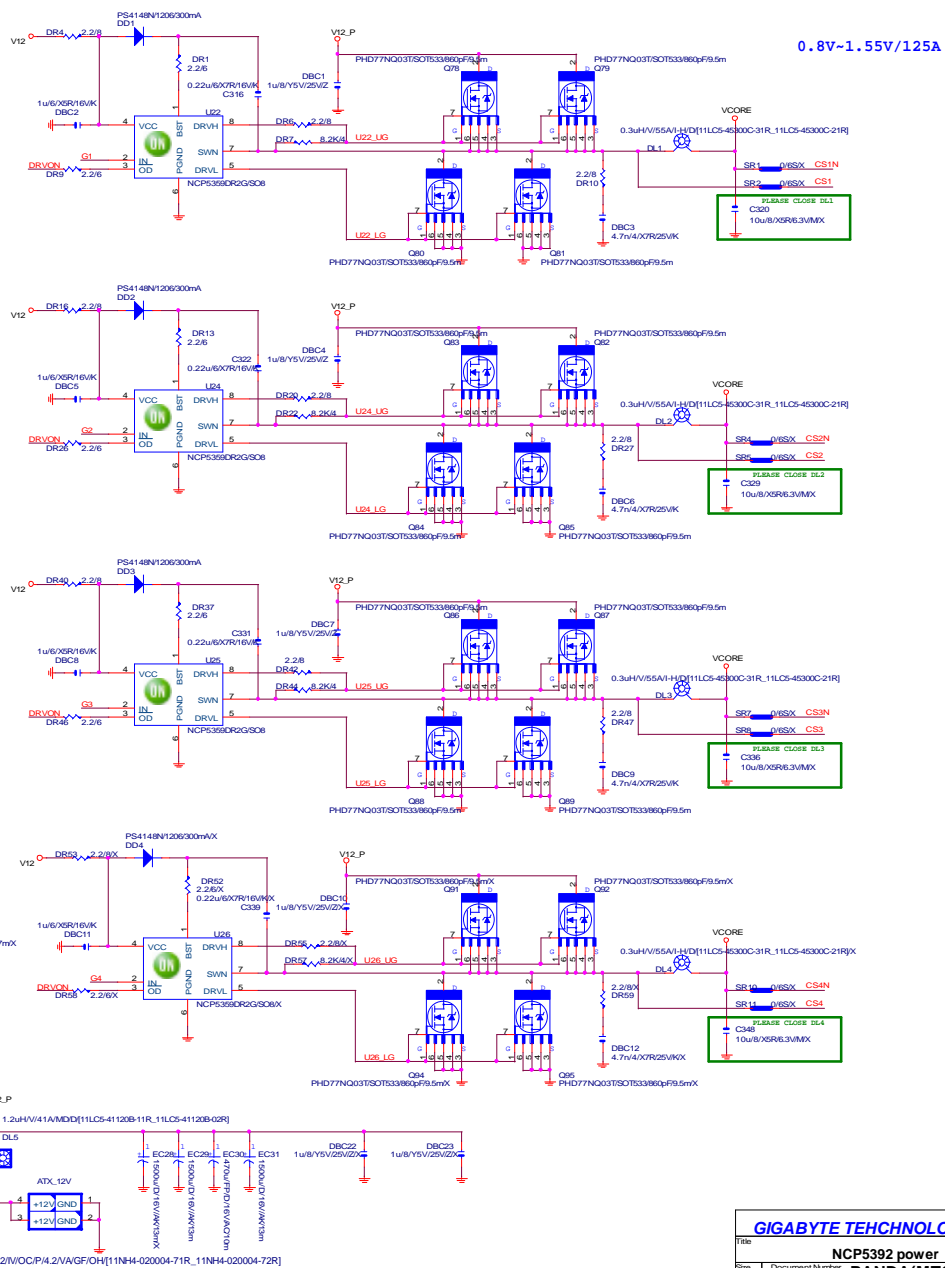


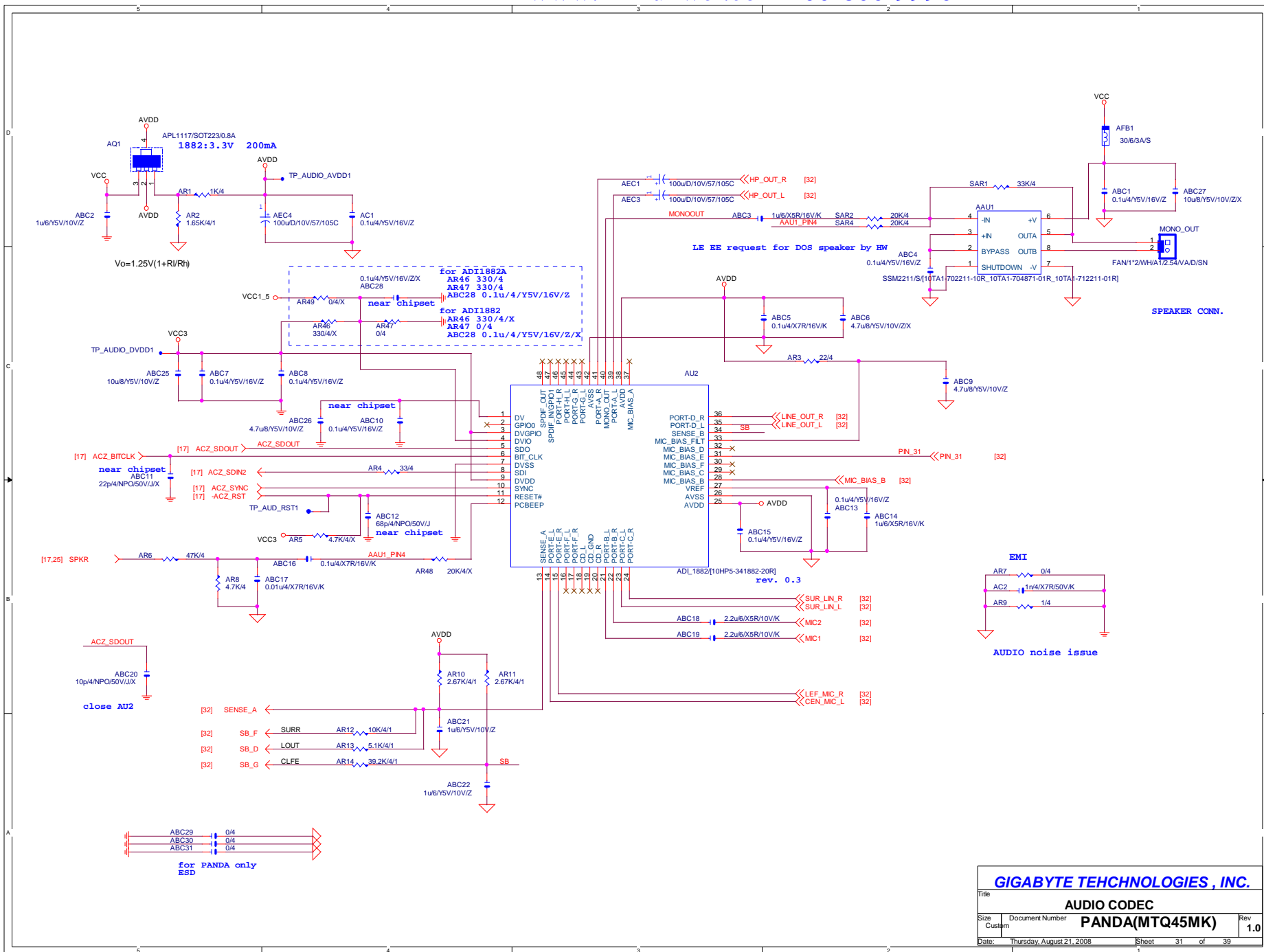
## VCC3\_CL



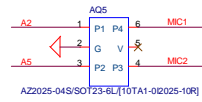
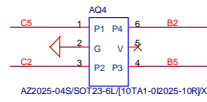
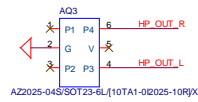
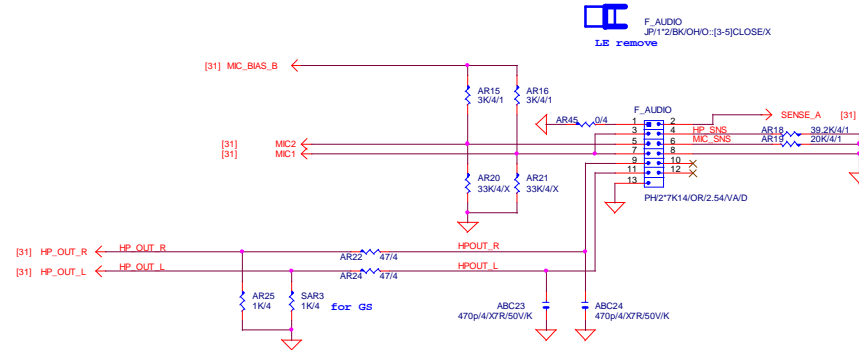
GIGABYTE TEHCHNOLOGIES, INC.

| Title          |                           |                |          |
|----------------|---------------------------|----------------|----------|
| DISCRETE POWER |                           |                |          |
| Size           | Document Number           | PANDA(MTQ45MK) | Rev      |
| Custom         |                           |                | 1.0      |
| Date:          | Thursday, August 21, 2008 | Sheet          | 29 of 39 |

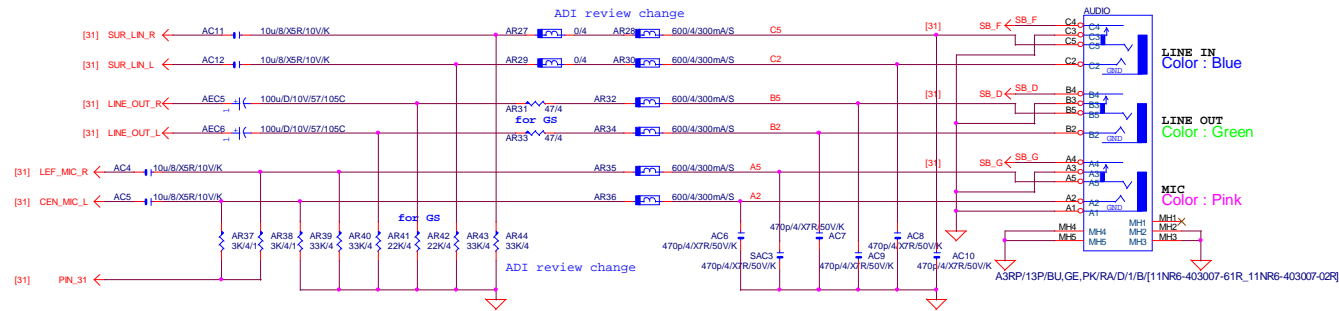




## FRONT AUDIO

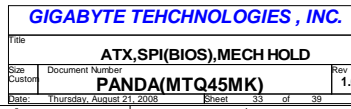


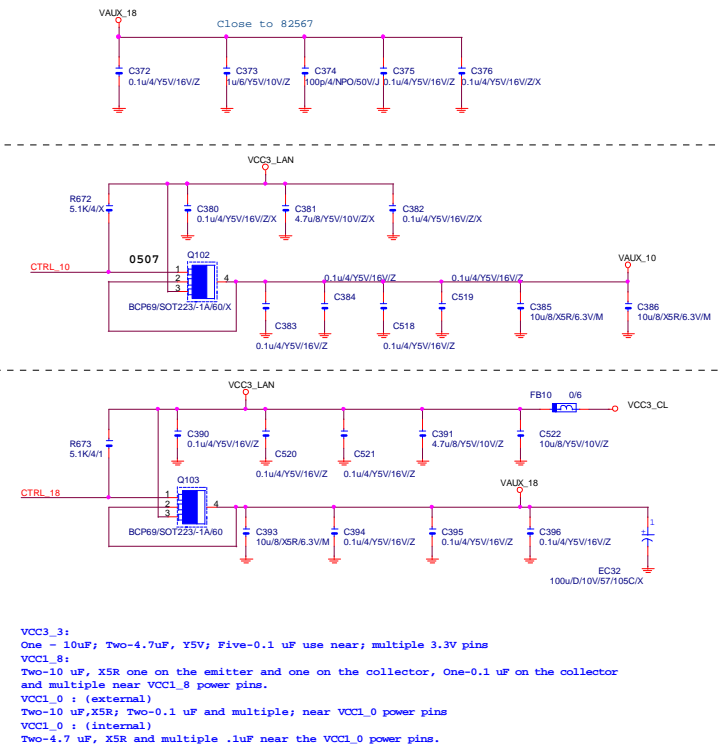
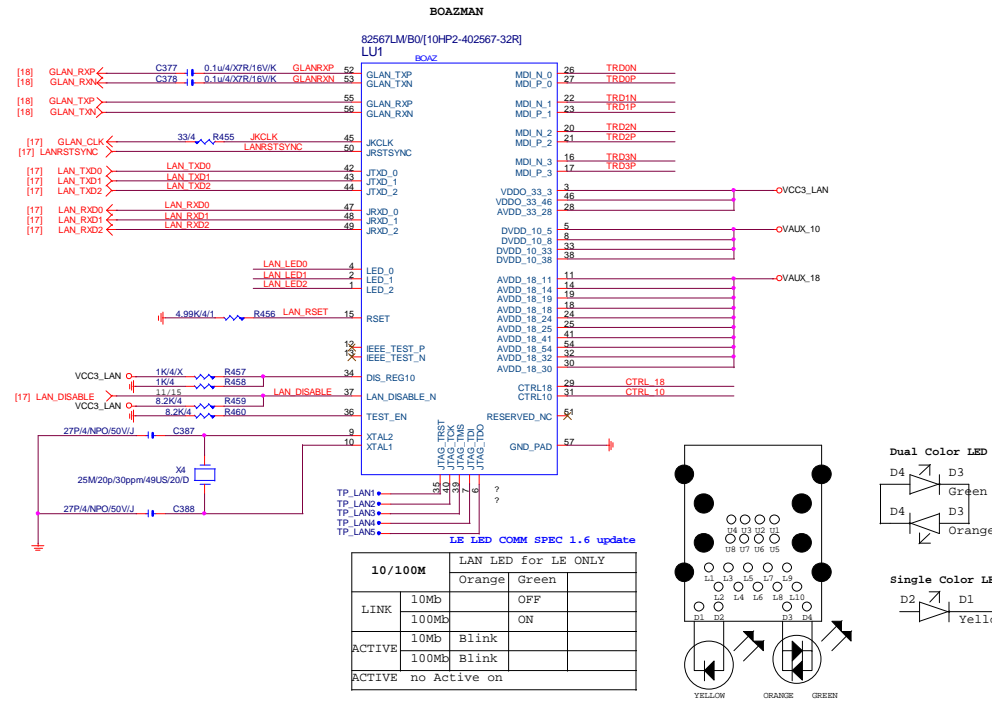
## AUDIO JACK

LINE IN  
Color : BlueLINE OUT  
Color : GreenMIC  
Color : Pink

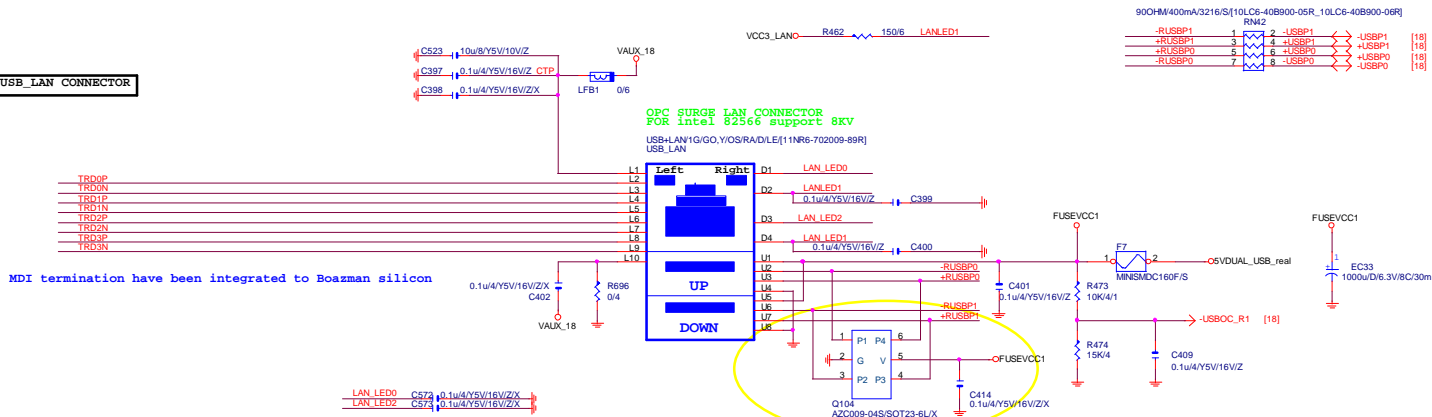
GIGABYTE TECHNOLOGIES, INC.

|            |                           |                |
|------------|---------------------------|----------------|
| AUDIO JACK |                           |                |
| File       | Document Number           | Rev            |
| Size       | PANDA(MTQ45MK)            | 1.0            |
| Date       | Thursday, August 21, 2008 | Sheet 32 of 39 |





**USB\_LAN CONNECTOR**



90CHW400mA/3216/S[10LC6-40B900-05R\_10LC6-40B900-08R]  
RMW2

|         |   |   |        |      |
|---------|---|---|--------|------|
| -RUSBP1 | 1 | 2 | -USBP1 | (18) |
| +RUSBP1 | 3 | 4 | +USBP1 | (18) |
| -RUSBP0 | 5 | 6 | -USBP0 | (18) |
| +RUSBP0 | 7 | 8 | +USBP0 | (18) |

|          | Status | Speed |       | Active |
|----------|--------|-------|-------|--------|
|          |        | Left  | Right |        |
| 10M/100M | 10Mb   | OFF   | Blink |        |
|          | 100Mb  | ON    | Blink |        |

|         | Status | Speed          |        | Active |
|---------|--------|----------------|--------|--------|
|         |        | Dual Color LED |        |        |
|         |        | Green          | Orange |        |
| Gigabit | 10Mb   | OFF            | OFF    | Blink  |
|         | 100Mb  | ON             | OFF    | Blink  |
|         | 1Gb    | OFF            | ON     | Blink  |

**GIGABYTE TECHNOLOGIES, INC.**

|        |                           |                |          |
|--------|---------------------------|----------------|----------|
| File   | intel GbE 82567LM BOAZMAN |                |          |
| Size   | Document Number           | PANDA(MTQ45MK) |          |
| Custom |                           | Rev            | 1.0      |
| Date   | Thursday, August 21, 2008 | Sheet          | 34 of 39 |

ICH10 GPIO TABLE

| GPIO    | Use Signal Name   | Power  | USE In/Out | ACTIVE H/L | Mark   | INTERNAL/EXTERNAL PULL HIGH / LOW |
|---------|-------------------|--------|------------|------------|--|-----------------------------------|
| GPIO_0  | ICH_BMBUSYB       | VCC3   | IN         | L          | SET Bus master busy from SST   | FORM ICH_GPT_BMBUSYB              |
| GPIO_1  | TACH_SYSFAN       | VCC3   | IN         | ---        | SYSTEM FAN speed detect  | EXT / HIGH                        |
| GPIO_2  | -PIRQE            | VCC3   | ---        | L          | PCI1 solt IRQA   | EXT / HIGH                        |
| GPIO_3  | -PIRQF            | VCC3   | ---        | L          | PCI2 solt IRQA   | EXT / HIGH                        |
| GPIO_4  | -PIRQG            | VCC3   | ---        | ---        | no use   | EXT / HIGH                        |
| GPIO_5  | -PIRQH            | VCC3   | ---        | ---        | no use   | EXT / HIGH                        |
| GPIO_6  | TACH_PWRFAN       | VCC3   | IN         | ---        | PWR FAN speed detect   | EXT / HIGH                        |
| GPIO_7  | ICH_GPIO7         | VCC3   | IN         | L          | POWER LED GREEN  | EXT / HIGH                        |
| GPIO_8  | DRAMPWROK         | 3VDUAL | Out        | H          | ICH to MCH   | EXT / HIGH                        |
| GPIO_9  | WOL_ONLY          | 3VDUAL | Out        | H          | enable LAN of power under S3-S5 if AMT or ASP diable   | EXT / HIGH                        |
| GPIO_10 | -SKTOCC           | 3VDUAL | IN         | L          | Detect CPU in socket<br>L=INSERT H=NO-INS DEFAULT=H  | EXT / HIGH                        |
| GPIO_11 | -SMBALRT          | 3VDUAL | IN         | ---        | no use   | EXT / HIGH                        |
| GPIO_12 | LAN_DISABLE       | 3VDUAL | Out        | H          | INTEL 82567L5/LM FUNCTION<br>L=ENABLE H=DISABLE DEFAULT=H  | EXT / HIGH                        |
| GPIO_13 | -LPCPME           | 3VDUAL | IN         | L          | LPC POWER MANAGEMENT EVEN  | EXT / HIGH                        |
| GPIO_14 | ICH_QST_BMBUSYB   | 3VDUAL | Out        | L          | SST Bus master busy arrange  | EXT / HIGH                        |
| GPIO_15 | -CK_PCI_STOP      | 3VDUAL | Out        | L          | set PCI clock to stop from clock gen for AMT mode<br>L=STOP PCI CLOCK H=ENABLE PCI CLOCK DEFAULT=H | NO NEED                           |
| GPIO_16 | ICH_GPO16         | VCC3   | Out        | L          | M/B ID2  | INT PULL / DOWN<br>EXT / HIGH     |
| GPIO_17 | TACH_CPUFAN       | VCC3   | IN         | ---        | CPU FAN speed detect   | EXT / HIGH                        |
| GPIO_18 | ICH_GPIO18        | VCC3   | OUT        | ---        | CONTROL GTLREF OFFSET  | EXT / HIGH                        |
| GPIO_19 | ICH_GPIO19        | VCC3   | IN         | H          | LPT USE  | EXT / HIGH                        |
| GPIO_20 | N/C               | VCC3   | OUT        | L          | no use FOR STRAP PIN<br>RESERVED STRAP (DON'T PULL-HIGH)   | INT PULL / DOWN<br>TP             |
| GPIO_21 | ICH_GPIO21        | VCC3   | IN         | H          | BIOS WP  | EXT / HIGH                        |
| GPIO_22 | ICH_GPIO22        | VCC3   | ---        | ---        | LEO CHIP USE   | EXT / HIGH                        |
| GPIO_23 | N/C               | VCC3   | ---        | ---        | no use   | INT PULL / HIGH<br>TP             |
| GPIO_24 | ICH_GPIO24        | 3VDUAL | OUT        | H          | PWR LED YELLOW   | EXT / HIGH                        |
| GPIO_25 | -CK_CPU_STOP      | 3VDUAL | OUT        | H          | set CPU clock to stop from clock gen for AMT mode<br>L=STOP CPU CLOCK H=ENABLE CPU CLOCK DEFAULT=H | NO NEED                           |
| GPIO_26 | -S4_STATE         | 3VDUAL | OUT        | ---        | -S4_STATE  | TP                                |
| GPIO_27 | ICH_GPO27         | 3VDUAL | IN         | L          | BIOS WRITE PROTECT<br>L=ENABLE H=DISABLE DEFAULT=H   | EXT / HIGH                        |
| GPIO_28 | TCM_DIS#_GPIO28   | 3VDUAL | Out        | L          | LEO_CHIP   | EXT / HIGH                        |
| GPIO_29 | -USBOC_R3         | 3VDUAL | IN         | L          | DETECT USB4,5 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H  | EXT / HIGH                        |
| GPIO_30 | -USBOC_F1         | 3VDUAL | Out        | L          | DETECT USB6,7 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H  | EXT / HIGH                        |
| GPIO_31 | -USBOC_F2         | 3VDUAL | Out        | L          | DETECT USB8,9 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H  | EXT / HIGH                        |
| GPIO_32 | ICH_GPO32         | VCC3   | Out        | H          | CLR_CMOS<br>H=ENABLE L=DISABLE DEFAULT=H   | EXT / HIGH                        |
| GPIO_33 | ICH_GPIO33        | VCC3   | IN         | ---        | ME_DISABLE<br>H=EFFECT L=OVERRIDE DEFAULT=H  | INT PULL / HIGH<br>EXT / HIGH     |
| GPIO_34 | TCM_FRSNT#_GPIO34 | VCC3   | Out        | L          | LEO_CHIP PRSNT   | EXT / HIGH                        |
| GPIO_35 | ICH_GPO35         | VCC3   | Out        | L          | CONTROL GTLREF OFFSET  | EXT / HIGH                        |
| GPIO_36 | ICH_GPIO36        | VCC3   | IN         | H          | F_USB1   | EXT / HIGH                        |
| GPIO_37 | ICH_GPIO37        | VCC3   | IN         | H          | F_USB2   | EXT / HIGH                        |
| GPIO_38 | ICH_GPIO38        | VCC3   | IN         | ---        | COMB   | EXT / HIGH                        |
| GPIO_39 | ICH_MBDIO         | VCC3   | IN         | ---        | M/B ID 0   | EXT / LOW                         |
| GPIO_40 | -USBOC_R1         | 3VDUAL | IN         | L          | DETECT USB0,1 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H  | EXT / HIGH                        |
| GPIO_41 | -USBOC_R2         | 3VDUAL | IN         | L          | DETECT USB2,3 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H  | EXT / HIGH                        |
| GPIO_42 | -USBOC_R3         | 3VDUAL | IN         | L          | DETECT USB4,5 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H  | EXT / HIGH                        |
| GPIO_43 | -USBOC_R4         | 3VDUAL | IN         | L          | DETECT USB6,7 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H  | EXT / HIGH                        |
| GPIO_44 | -USBOC_F2         | 3VDUAL | IN         | L          | DETECT USB8,9 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H  | EXT / HIGH                        |
| GPIO_45 | -USBOC_F2         | 3VDUAL | IN         | L          | DETECT USB8,9 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H  | EXT / HIGH                        |
| GPIO_46 | N/C               | 3VDUAL | ---        | ---        | NO USE PUSH HIGH   | EXT / HIGH                        |
| GPIO_47 | N/C               | 3VDUAL | ---        | ---        | NO USE PUSH HIGH   | EXT / HIGH                        |
| GPIO_48 | ICH_MBD1          | VCC3   | IN         | ---        | M/B ID 1   | EXT / LOW                         |
| GPIO_49 | GPIO49            | VCC3   | OUT        | H          | DMI HALF/PULL AWING STRAP<br>FOR EAGLELAKE = HIGH (EMPTY) HALF                                     | INT PULL / HIGH                   |

| GPIO    | Use Signal Name | Power  | USE In/Out | ACTIVE H/L | Mark  | INTERNAL PULL HIGH / LOW |
|---------|-----------------|--------|------------|------------|---|--------------------------|
| GPIO_50 | -REQ1           | VCC    | ---        | L          | FOR PCI SOLT1 REQ SIGNAL                                    | EXT / HIGH               |
| GPIO_51 | -GNT1           | VCC3   | Out        | L          | FOR PCI SOLT1 GNT SIGNAL<br>RESERVED STRAP ,NOT PULL LOW    | INT PULL / HIGH          |
| GPIO_52 | -REQ2           | VCC    | ---        | ---        | NO USE PUSH HIGH  | EXT / HIGH               |
| GPIO_53 | -GNT2           | VCC3   | ---        | ---        | NO USE<br>PCIe PORT C0FIG 2 STRAP                           | INT PULL- HIGH           |
| GPIO_54 | -REQ3           | VCC    | ---        | ---        | NO USE PUSH HIGH  | EXT / HIGH               |
| GPIO_55 | -GNT3           | VCC3   | ---        | ---        | NO USE<br>TOP-BLOCK SWAP OVERRIDE STRAP                     | INT PULL- HIGH           |
| GPIO_56 | ICH_GPIO56      | 3VDUAL | IN         | ---        | BIOS WP   | EXT / HIGH               |
| GPIO_57 | ITPM_PP_ICH     | 3VDUAL | IN         | ---        | INTERNAL TPM FUNCTION<br>STRAP H=ENABLE L=DISABLE DEFAULT=H | EXT / HIGH<br>EXT / LOW  |
| GPIO_58 | -SPI_CS1_C      | 3VDUAL | IN         | ---        | WITH GNT0 SELETC BIOS TYPE STRAP                            | INT PULL- HIGH           |
| GPIO_59 | -USBOC_R1       | 3VDUAL | IN         | L          | DETECT USB0,1 POWER OC<br>L=OC OCCUR H=FREE DEFAULT=H       | EXT / HIGH               |
| GPIO_60 | -LINKALERT      | 3VDUAL | ---        | ---        | NO USE PUSH HIGH  | EXT / HIGH               |
| GPIO_61 | -LPCPD          | 3VDUAL | OUT        | L          | LPC DEVICE POWER DOWN<br>L=ENABLE H=DISABLE DEFAULT=H       | EXT / HIGH               |
| GPIO_62 | SPSCLK          | 3VDUAL | ---        | ---        | no use  | TP                       |
| GPIO_63 | -SLP_S5         | 3VDUAL | ---        | ---        | no use  | TP                       |
| GPIO_72 | ICH_MBD12       | VCC3   | ---        | ---        | no use  | TP                       |

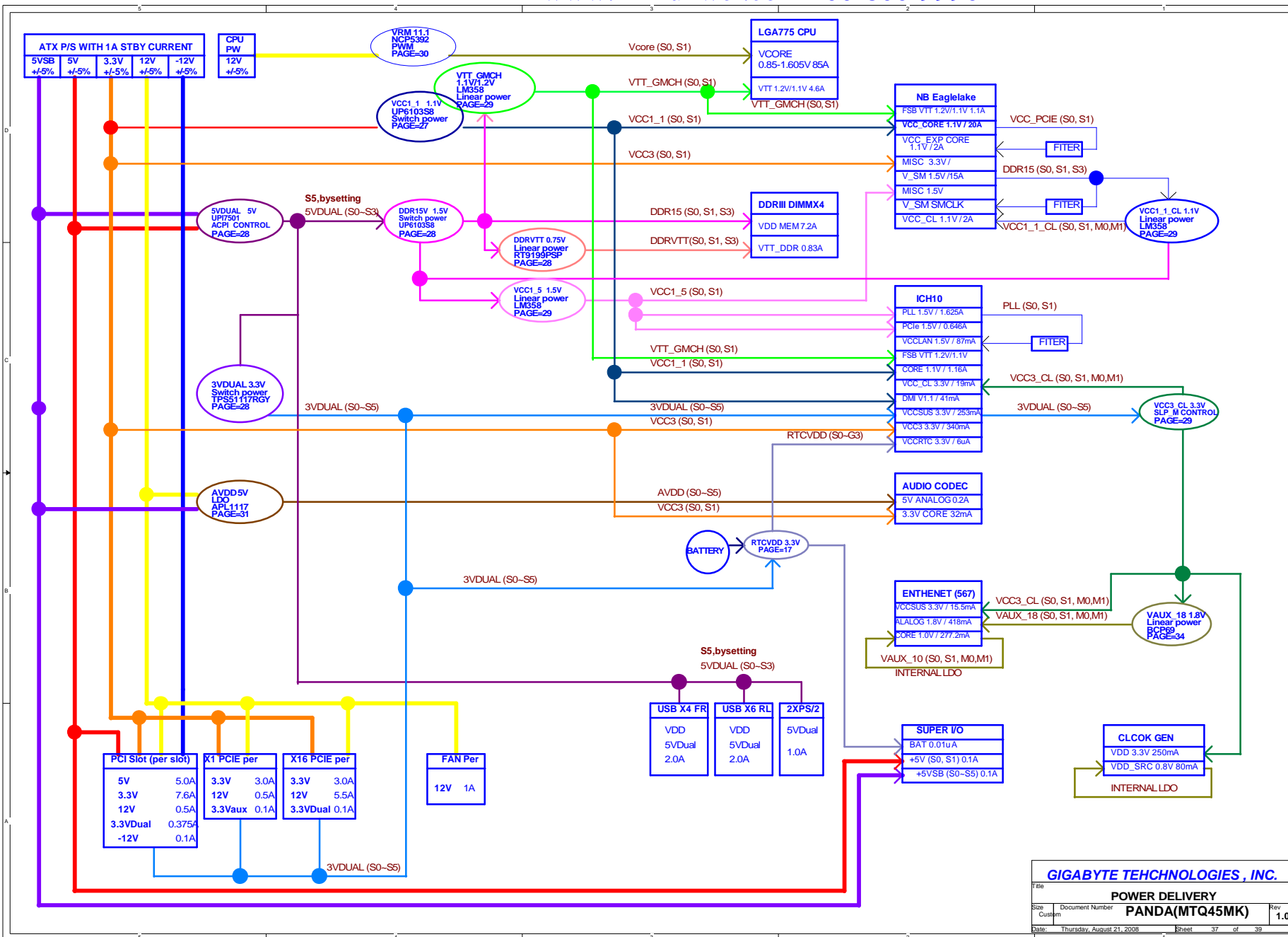
EAGLELAKE PLATFORM STRAP LIST

| Use Signal Name                              | Usage                                       | When Sample                           | Comment  |
|--|---|---------------------------------------|--|
| HDA_SDOUT_TP3<br>INT PULL/DOWN INT PULL/HIGH | XOR Chain Entrance                          | Rising Edge of PWROK                  | Allows entrance to XOR chain testing   |
| ---  | L   |                                       |  |
| L  | H   |                                       |  |
| H  | H   |                                       |  |
| -SATALED                                     | PCIe 1x4 lane reversal<br>only for consumer | Rising Edge of PWROK                  | Chipset Config Registers :offset 224h  |
| HDA_SYNC                                     | Set PCIe port 1x4 lane<br>only for consumer | Rising Edge of PWROK                  | If HDA_SDOUT=H HDA_SYNC=H<br>-SATALED =H disable Default<br>set PCIe=1x4 P0:LAYOUT NOT IMPLEMENT   |
| -GNT2  | DMI Clock Data Enable                       | Rising Edge of PWROK                  | collocate with HDA_SDOUT<br>HDA_SDOUT=H HDA_SYNC=H<br>L,R or H,L reserved P0:LAYOUT NOT IMPLEMENT  |
| -GNT1  | DMI Clock Data Enable                       | Rising Edge of PWROK                  | FWC_PCIE offset 0224 bit 0:1 BIOS must program field 11b<br>H= Enable default<br>L= Disable  |
| -GNT3  | Top Block Swap Override                     | Rising Edge of PWROK                  | ICH10 invertes A16 for all cycles targeting BIOS spaces<br>H= Enable default<br>L= Disable   |
| -GNT0  | -SPI_CS1_C                                  | boot BIOS Destination selection       | If option LPC is selected BIOS may still be placed on LPC<br>but all platforms with ICH10(Corporate only) require<br>SPI flash connected directly to the SPI bus with a valid<br>descriptor in order to boot |
| L  | H   |                                       |  |
| H  | L   |                                       |  |
| H  | H   |                                       |  |
| TP20   | Reserved                                    | Rising Edge of PWROK                  | RESERVED STRAP (DON'T PULL-HIGH)   |
| INT PULL/LOW                                 | SPKR  | No Reboot                             | ICH10 will control the TCO timer system reboot feature.<br>H= Enable<br>L= Disable default   |
| INT PULL/HIGH                                | ICH_GPIO33                                  | Flash Descriptor Security<br>Override | Low , the flash Descriptor security overrides<br>HIGH , the flash Descriptor security effect<br>H= Enable default L= Disable   |
| GPIO49                                       | DMI Termination Voltage                     | Rising Edge of PWROK                  | FOR BL=LOW<br>FOR EAGLELAKE = HIGH (EMPTY) HALF<br>H= Half Swing default L= Full Swing   |
| SPI_MOSI_C                                   | Integrated TPM (for ICH10)                  | Rising Edge of CLPWROK                | H= Enable<br>L= Disable default  |
| ITPM_EN                                      | Integrated TPM (for QMCH)                   | Rising Edge of PWROK                  | H= Disable default<br>L= Enable  |
| DDPC_CTRLDATA                                | Enable Digital port C                       | Rising Edge of PWROK                  | H= Enable L= Disable   |
| SDVO_CTRL_DATA                               | Enable Digital port B                       | Rising Edge of PWROK                  | H= Enable L= Disable   |
| EXP_SLR                                      | PCI Express Static Lane Reversal            | Rising Edge of PWROK                  | For BTX platform need reversed<br>L= lane reversed H= Normal Default   |
| -PEG_PRSNT2                                  | Concurrent SDVO and PCI Express             | Rising Edge of PWROK                  | H= Both SDVO and PCI Express<br>L= Only SDVO or PCI Express  |
| CEN  | TLS confidentiality                         | Rising Edge of PWROK                  | Support AMT need enable<br>H= Disable TLS L= Enable TLS  |
| DUALX8_EN                                    | 2x8 PEG port Bifurcation                    | Rising Edge of PWROK                  | H= 1x16 PCIe Port<br>L= 2x8 PCIe Ports   |
| -PEG_PRSENCE                                 | Enable Eaglelake PEG                        | Rising Edge of PWROK                  | H= Enable PEG out<br>L= PCIe x16 insert  |

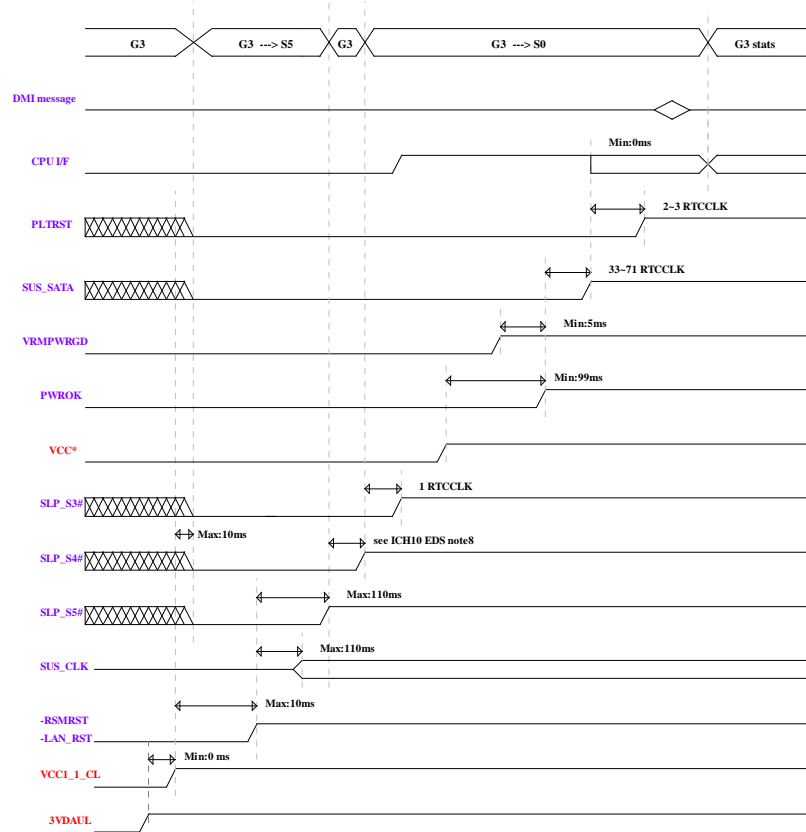
GIGABYTE TECHNOLOGIES, INC.

File Eaglelake & ICH10 for GPIO & Strap  
 Docu Document Number: PANDA(MTQ45MK)  
 Rev 1.0  
 Date Thursday, August 11, 2016 Page 35 of 35





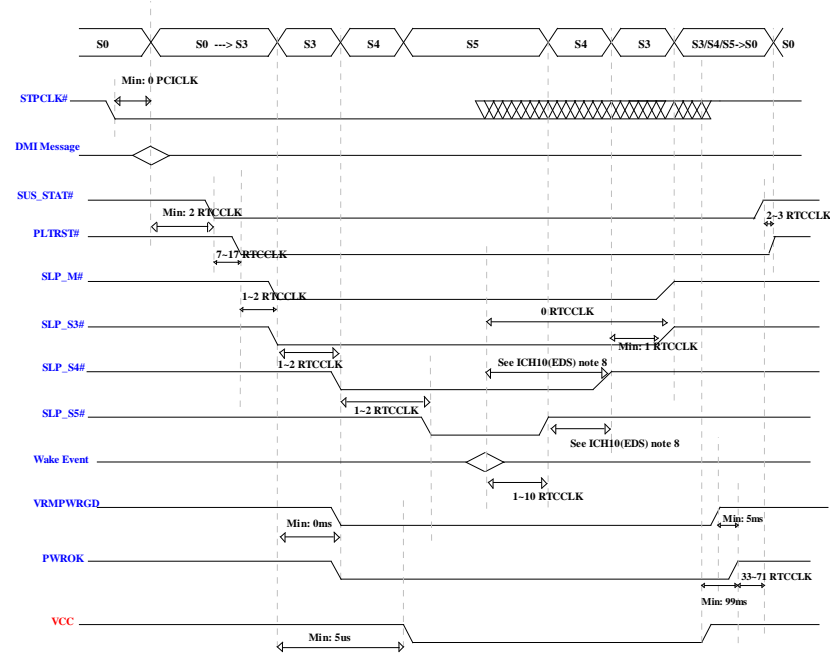
## G3-tO-S0 Power Sequence



Power Planes in Red Motherboard generated signals in Purple

VCC\* includes VCCL1\_5 VCC3 VCCL1 VTT\_GMCH VREF

## S0 to S5 to S0 Timings



Power Planes in Red Motherboard generated signals in Purple

VCC\* includes VCCL1\_5\_A VCCL1\_5\_B VCC3\_3 VCCL1 VCCUSBPLL VCCDMIPLL VCCSATAPLL

[illegible]